WG0501C

Datasheet

Dual Channel High-Speed and Low-Side Driver WG0501C

Features

- Two Independent Gate Drive Channels
- 4.5Vto18V Single Supply Range
- CMOS Input Logic Threshold
- 5A Peak Source and 5A Peak Sink Symmetrical Drive
- Fast Propagation Delays
- Fast Rise and Fall Times
- Output Held Low when Input Pins are Floating
- Hysteresis-Logic Thresholds for High Noise Immunity
- Ability to handle negative voltage(-5V)at input
- SOP-8L Package

Description

The WG0501C device is a high-speed dual-channel, low-side gate driver device. It is a dual non-inverting driver, and is capable of effective driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, WG0501C is capable of sourcing and sinking high,peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13ns.

The WG0501C provide 5A source, 5A sink peak-drive current capability at V_{DD}=12V.

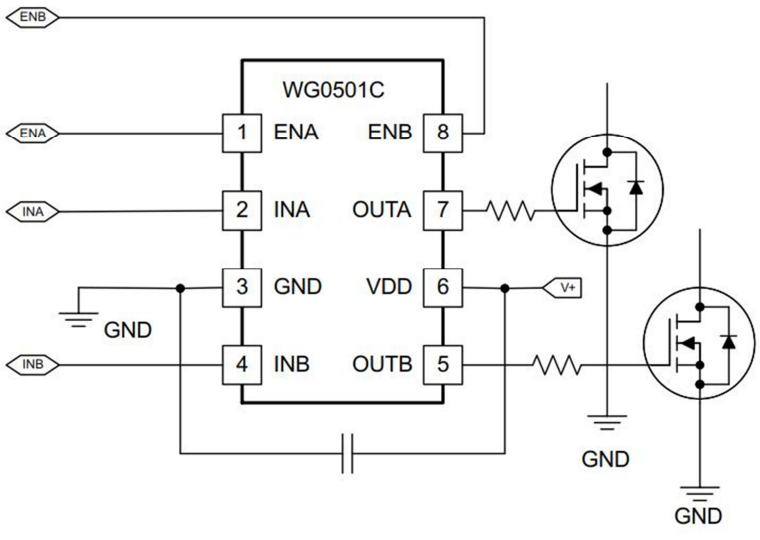
In addition, the drivers feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous retifier. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with a single input signal. The input pin thresholds are based on TTL and COMS compatible low-voltage logic, which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

The WG0501C is designed to operate over a wide VDD range of 4.5V to 18V and wide temperature range of -40°C to 140°C. Internal Under Voltage Lockout (UVLO) circuitry on V_{DD} pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power semiconductor devices.

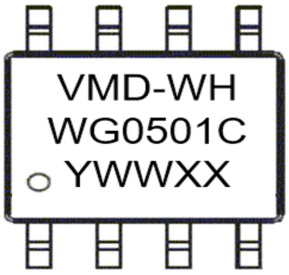
Applications

- Switch-Mode Power Supplies
- DC-DC Converters
- Companion Gate Driver Devices for Digital Power Controllers
- Solar Power, Motor Control, UPS
- Gate Driver for Emerging Wide Band-Gap Power Devices such as GaN

Typical Application Circuit

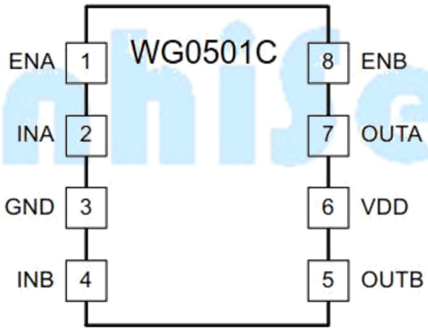


Ordering and Marking Information

Part Number	Marking Code	Package
WG0501C	 VMD-WH=Logo WG0501C=Device code XXXXX= Special code	**SOP-8L**

Pin Configuration

SOP-8L(TOP VIEW)



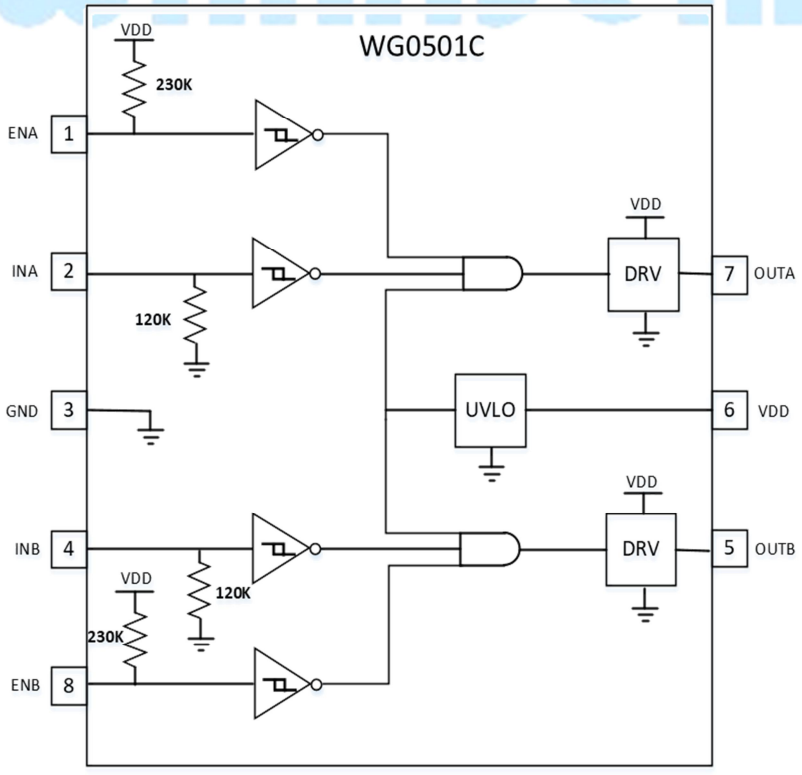
Pin Description

Pin No.	Name	Pin Function
1	ENA	ENA biased Low disables output regardless of Input state, ENA biased high or floating enables output, ENA is allowed to float.
2	INA	Non-inverting input in the WG0501C, output is held Low and is unbiased or floating.
3	GND	IC Ground Pin
4	INB	Non-inverting input in the WG0501C, output is held Low and is unbiased or floating.
5	OUTB	Output of Channel B
6	VDD	Power supply input.
7	OUTA	Output of Channel A
8	ENB	ENB biased Low disables output regardless of Input state, ENB biased high or floating enables output, ENB is allowed to float.

Absolute Maximum Values

Parameter	Symbol	Value	Unit
Supply Voltage(VDD)	VDD	-0.3 to 20.0	V
OUT Voltage	OUTA,OUTB	-0.3~VDD+0.3	V
Output Current(pulsed)		5	A
Output Current(continuous)		0.3	A
INA,INB,ENA,ENB Voltage	INA,INB,ENA,ENB	-0.3~20	V
ESD Human Body Rating		±4000	V
ESD,Charged Device Rating		±1000	V
Lead Temperature(soldering,10sec)		230	℃
Junction Temperature		150	℃
Storage Temperature		-65 to 150	℃

Block Diagram



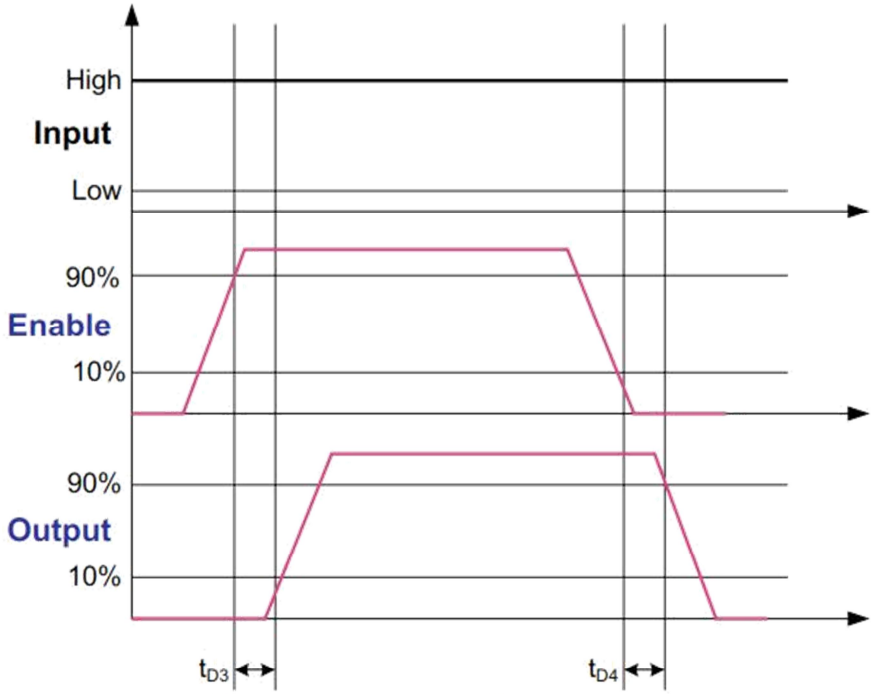
Electrical Characteristics (T_A= 25 ºC, V_{DD} = 12.0V,1uF capacitor from V_{DD} to GND)

Parameter	Symbol	Condition		Min	Typ	Max	Units
BIAS Currents							
Startup current	$I_{DD(off)}$	V_{DD}=3.4 V	INA,INB= V_{DD}	55	101	175	μA
			INA,INB = GND	20	55	125	
Under Voltage Lockout (UVLO)							
Supply start threshold	V_{ON}	T_A = 25°C		3.91	4.2	4.5	V
		T_A = -40°C to 140°C		3.7	4.2	4.65	
Minimum operating voltage after supply start	V_{OFF}			3.4	3.9	4.4	
Supply voltage hysteresis	V_{DD_H}			0.2	0.3	0.5	
INPUTS (INA,INB)							
Input signal high threshold	V_{IN_H}	Output high for non-inverting input pins		1.9	2.1	2.3	V
		Output low for inverting input pins					
Input signal low threshold	V_{IN_L}	Output high for non-inverting input pins		1	1.2	1.4	
		Output low for inverting input pins					
Input signal hysteresis	V_{IN_HYS}				0.9		
OUTPUTS(OUTA,OUTB)							
High output voltage	V_{DD}-V_{OH}	C_{LOAD}=0.22μF Fsw =1kHz			±5		A
High output voltage	V_{OH}	I_{OUT} = -10mA			0.25		V
Low output voltage	V_{OL}	I_{OUT} = 10mA			0.05		V
Output pull-up resistance	R_{OL}	I_{OUT} = -10mA			2.5		Ω
Output pull-down resistance	V_{OL}	I_{OUT} = 10mA			0.5		Ω

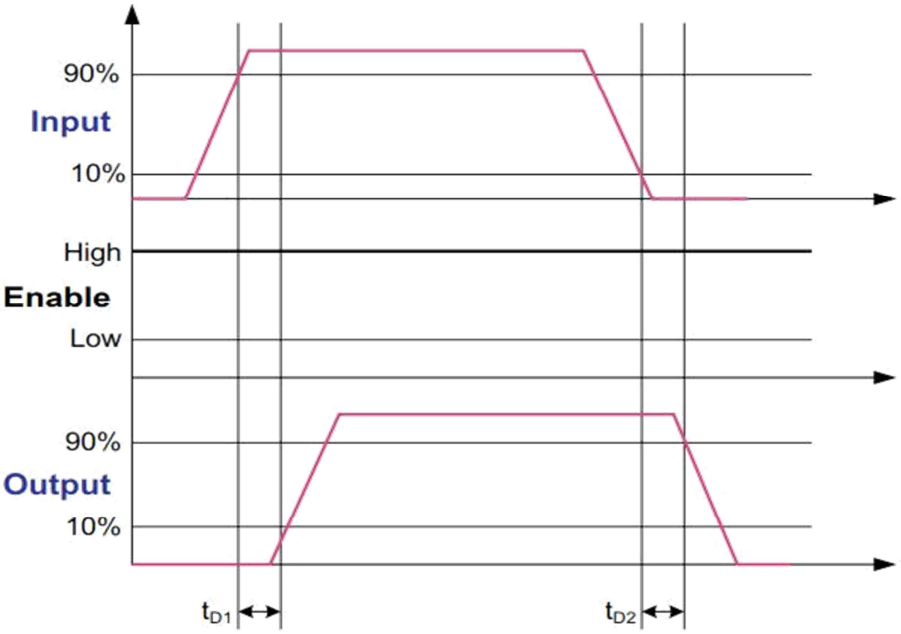
Switching Characteristics (V_{DD}=12V, over operating free-air temperature range)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Rise time	t_R	C_{LOAD}= 1.8nF		6		ns
Fall time	t_F	C_{LOAD}= 1.8nF		7		
Delay matching between 2 channels	t_M	INA=INB, OUTA=OUTB at 50% transition point		1		
Minimum input pulse width that changes the	t_{PW}			15		
Input to output propagation delay	t_{D1}	C_{LOAD}= 1.8nF, 5V input pulse		8		
	t_{D2}	C_{LOAD}= 1.8nF, 5V input pulse		9		
EN to output propagation delay	t_{D3}	C_{LOAD}= 1.8nF, 5V enable pulse		8		
	t_{D4}	C_{LOAD}= 1.8nF, 5V enable pulse		9		

Note: See the Enable Fuction figure, Test condition Enable from 10% to 90%.
See the Input Driver Operation figure, Test condition Input from 10% to 90%.



Enable Function



Input Driver Operation

Typical Performance Characteristics

Fig.1 Operating Supply Current vs Frequency

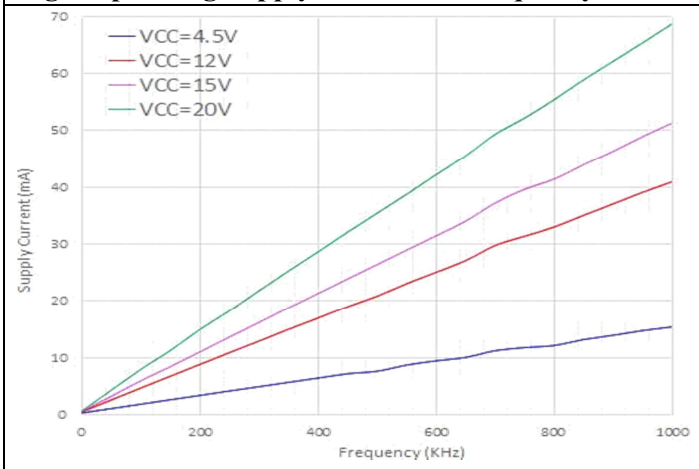


Fig.2 Propagation Delay vs Supply Voltage

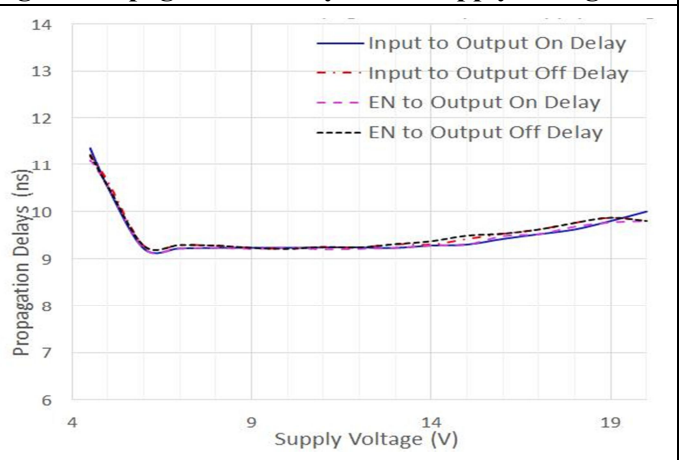


Fig.3 Rise Time vs Supply Voltage

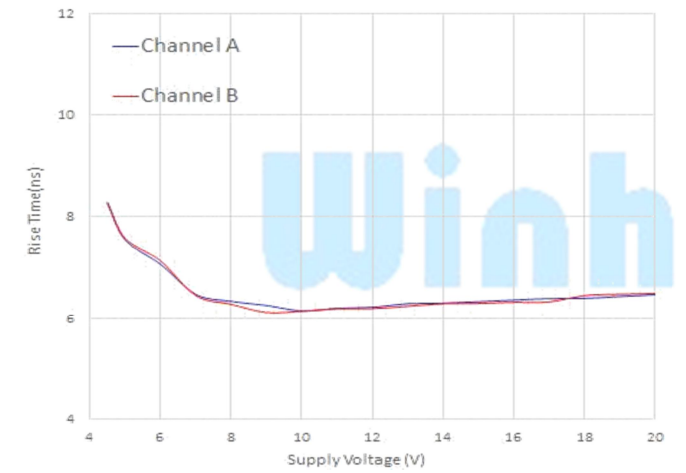


Fig.4 Fall Time vs Supply Voltage

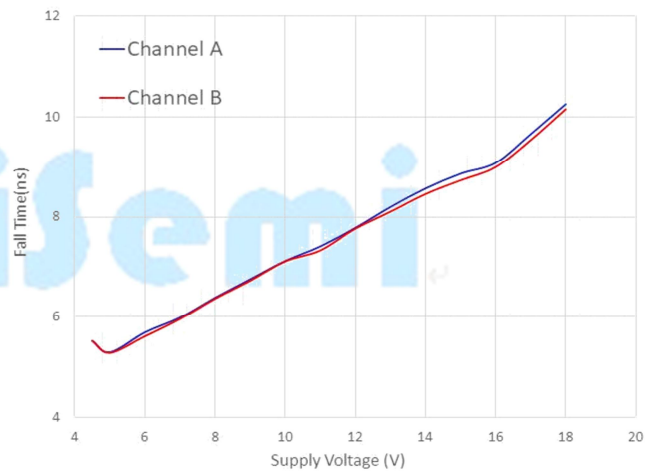


Fig.5 Start-Up Current vs Temperature

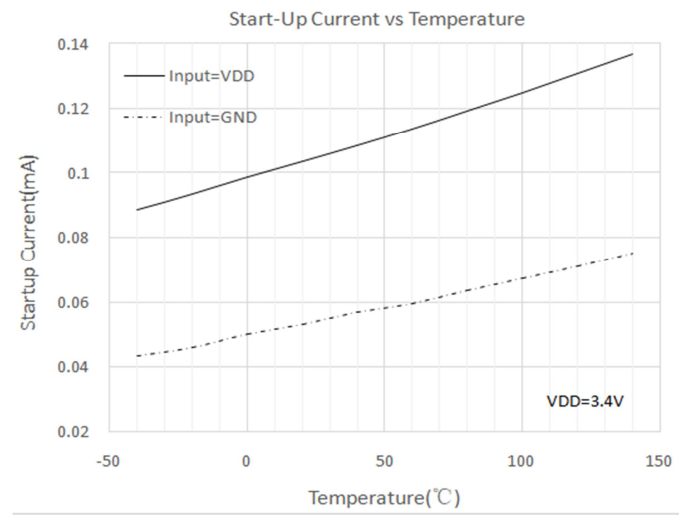


Fig.6 Operating Supply Current vs Temperature(Output Switching)

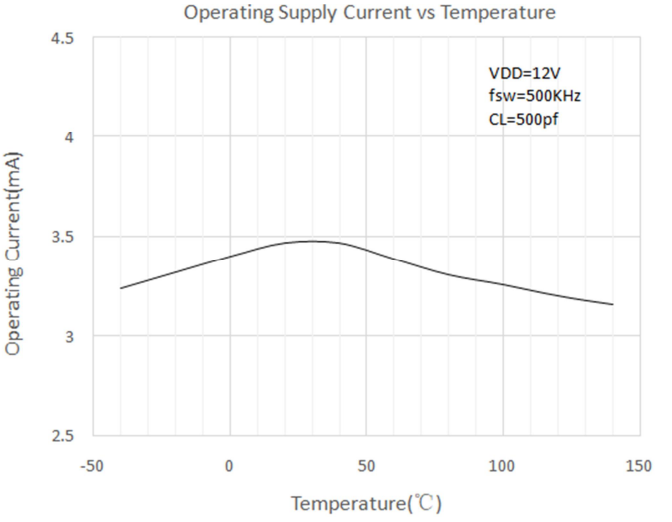


Fig.7 Operating Supply Current vs Temperature(Output in DC On/Off Condition)

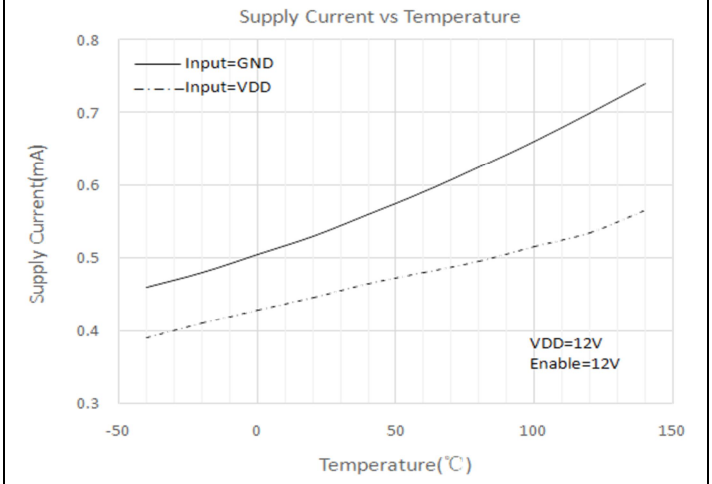


Fig.8 UVLO Threshold vs Temperature

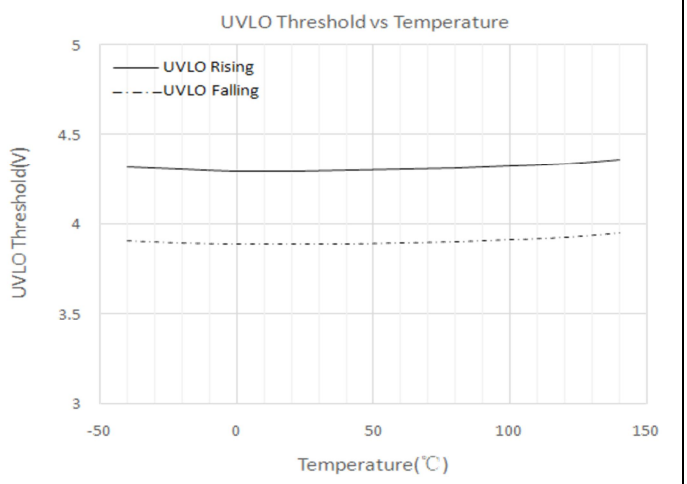


Fig.9 Input Threshold vs Temperature

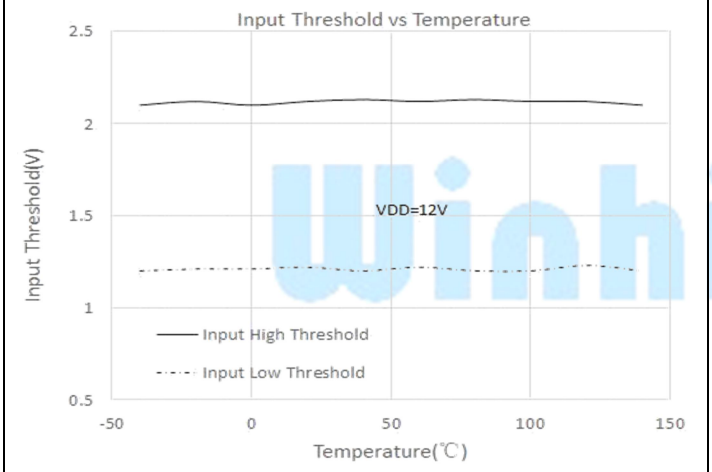


Fig.10 Rise Time vs Temperature

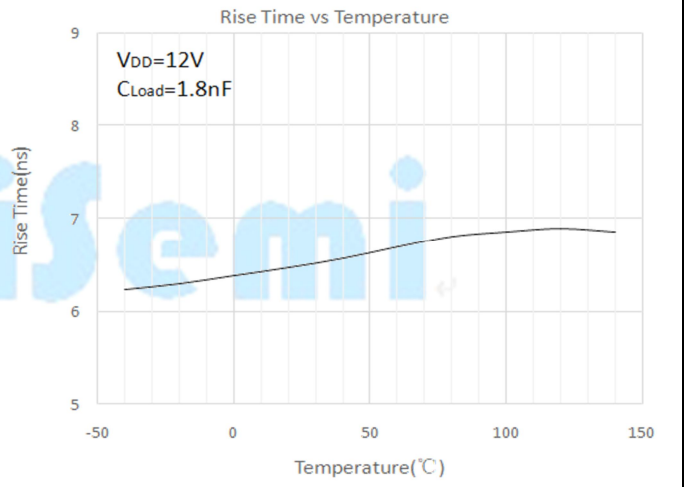


Fig.11 Fall Time vs Temperature

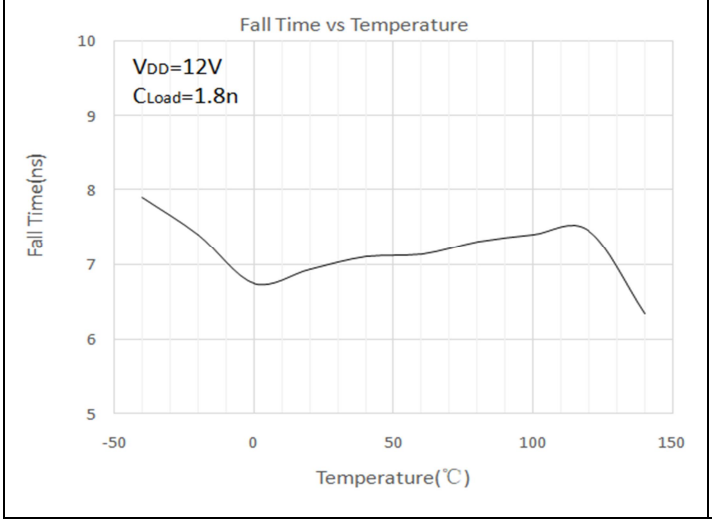


Fig.12 Input to Output Propagation Delay vs Temperature

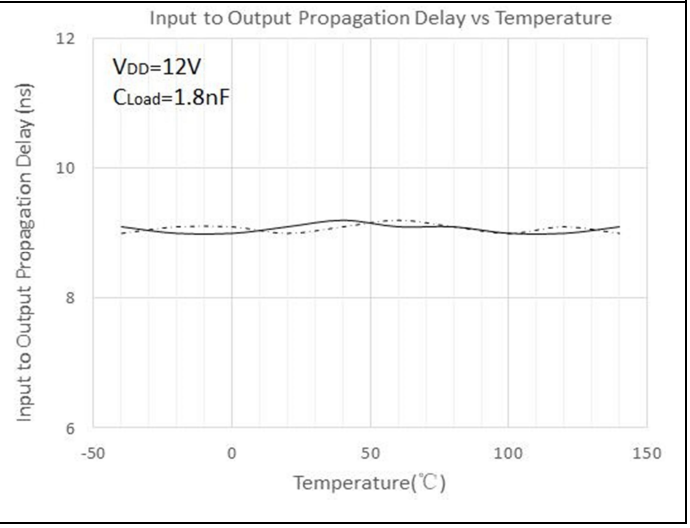


Fig.13 EN to Output Propagation Delay vs Temperature

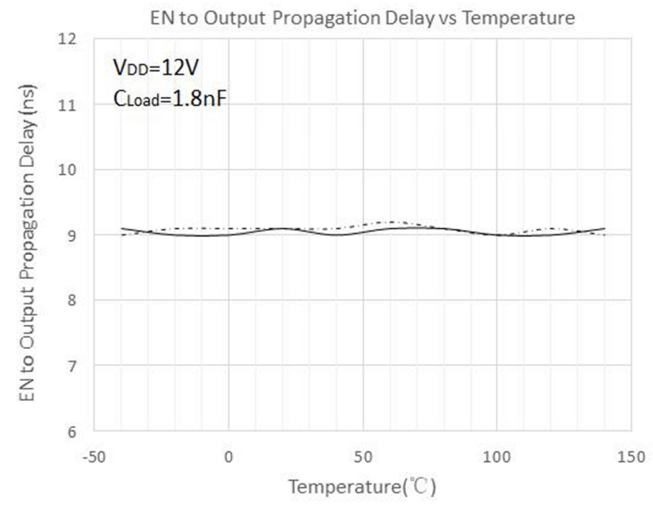


Fig.14 Output Pull up Resistance vs Temperature

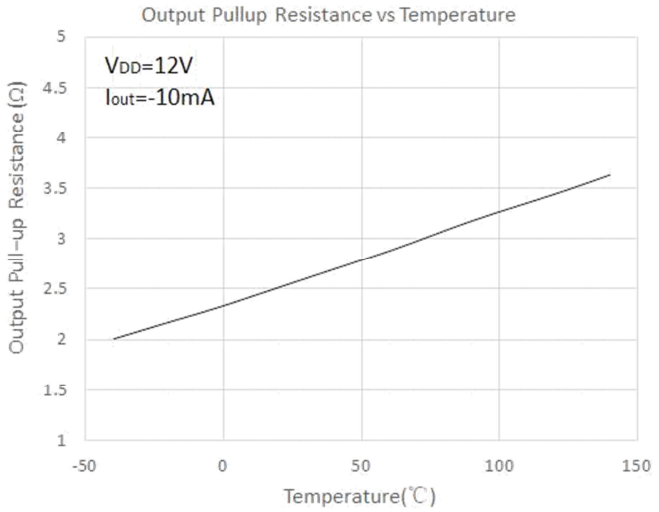


Fig.15 Output Pull Down Resistance vs Temperature

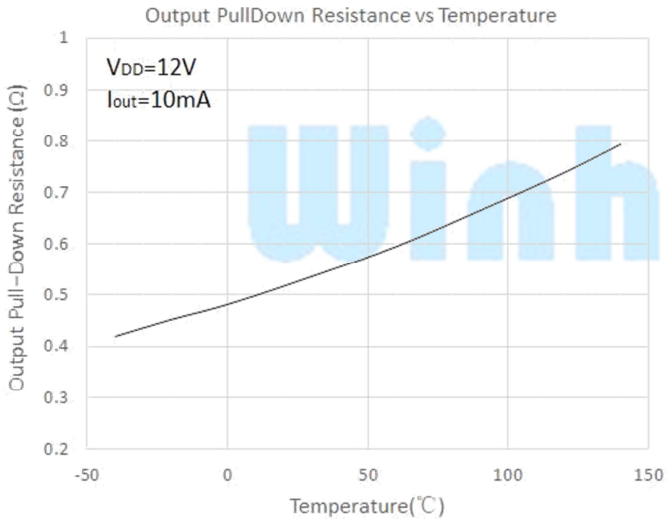
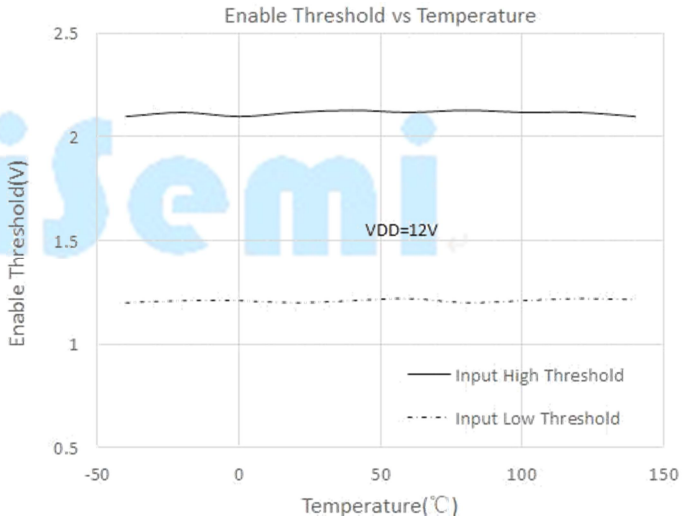


Fig.16 Enable Threshold vs Temperature



Application Information

The WG0501C device is a high-speed dual-channel, low-side gate driver device.It is a dual non-inverting driver, and is capable of effective driving MOSFET and IGBT power switches.Using a design that inherently minimizes shoot-through current, WG0501C is capable of sourcing and sinking high,peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13ns.

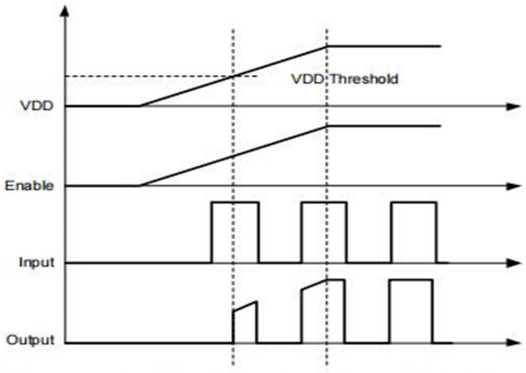
Supply Voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of WG0501C when driving very large MOSFETs. The minimum operating supply voltage is set by the under voltage lockout function to a typical default value of 4.2 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

The WG0501C device provides 5A source, 5A sink peak-drive current capability.The bias supply voltage range for which the WG0501C device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal under voltage-lock out protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VON supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the VDD pin of the device. Keeping a 2V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18 V. It is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

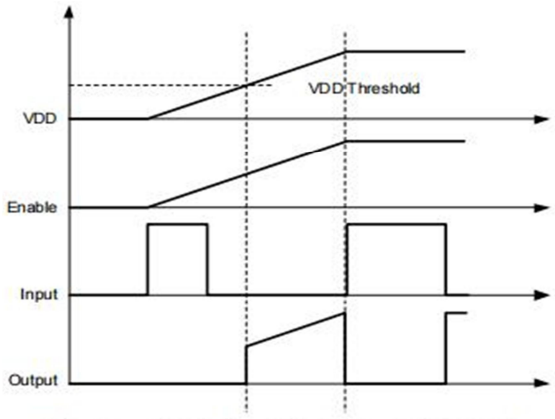
Under-Voltage Lockout (UVLO)

The Under Voltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 4.2V(with hysteresis). UVLO of 4.2 V is normally used for logic level based MOSFETs.



Power-up in a Non-Inverting Driver Channel

The WG0501C device follows non-inverting logic. The input pins of the devices are based on what is known as CMOS input threshold logic. In CMOS input logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. This offers the benefits of higher noise immunity due to the higher threshold voltage , as well as the ability to accept slow dv/dt input signals for manipulating the propagation delay between the PWM controller signal and the gate driver output. For system robustness, internal pull-up and pull-down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition.



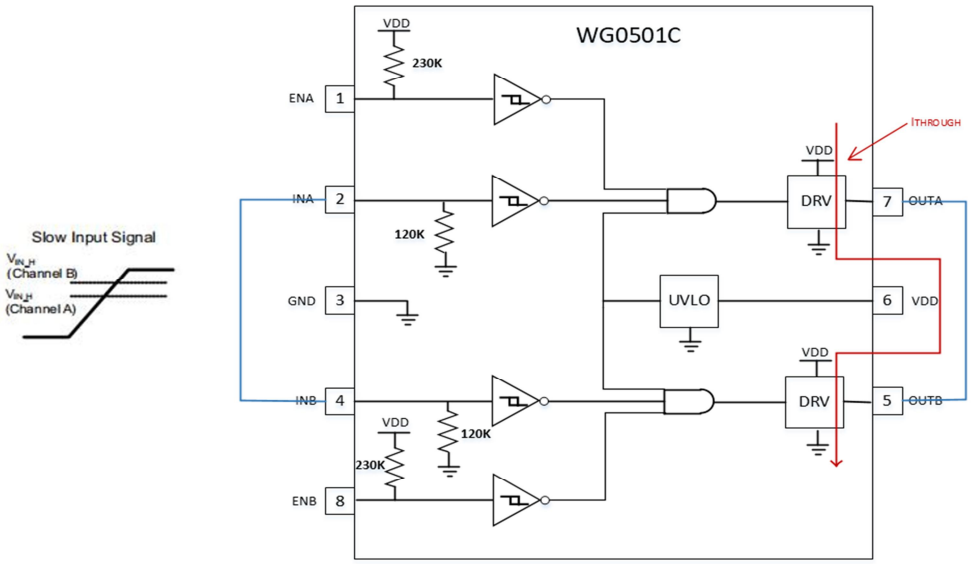
Power-up in an Inverting Driver Channel

Driver Outputs

In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. High-current gate driver devices are required in switching power applications for a variety of reasons. Emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low V_{DD} voltages, low propagation delays and availability in compact, low-inductance packages with good thermal capability.

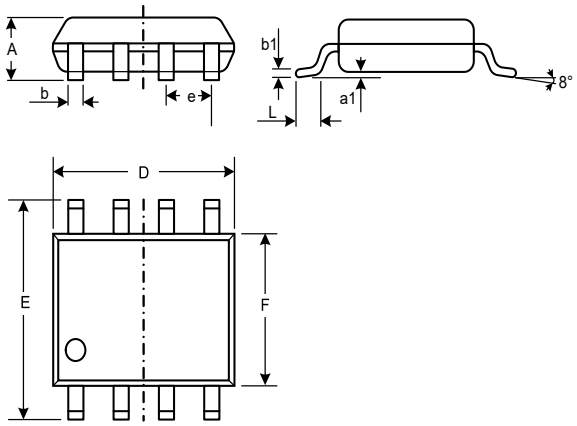
The WG0501C device features an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pull down resistors on all the non-inverting input pins .The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in WG0501C definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design



Mechanical Dimensions :

Package Information for SOP-8L



SYMBOL	MILLIMETER	
	MIN	MAX
A	1.23	1.75
a1	0.05	0.25
b	0.31	0.51
b1	0.16	0.25
D	4.7	5.15
E	5.75	6.25
e	1.07	1.47
F	3.7	4.1
L	0.4	1.27

Note:

1. Followed from JEDEC MO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 10mil per si.
3. A is the sum of A1and A2, and the overall height of the product.

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