WinhiSemi

WG0502A

Datasheet

Single Channel High-Speed and Low-Side Gate Driver WG0502A

Features

- Low-Cost Gate Drive Channel
- 4.5Vto18V Single Supply Range
- CMOS Input Logic Threshold
- 5A Peak Source and 5A Peak Sink Symmetrical Drive
- Fast Propagation Delays
- Fast Rise and Fall Times
- Output Held Low when Input Pins are Floating
- Hysteretic Logic Thresholds for High Noise Immunity
- SOT23-5L Package

Description

The WG0502A single-channel, high-speed, low-side gate driver device is capable of effective driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, The WG0502A is capable of sourcing and sinking high, peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13ns.

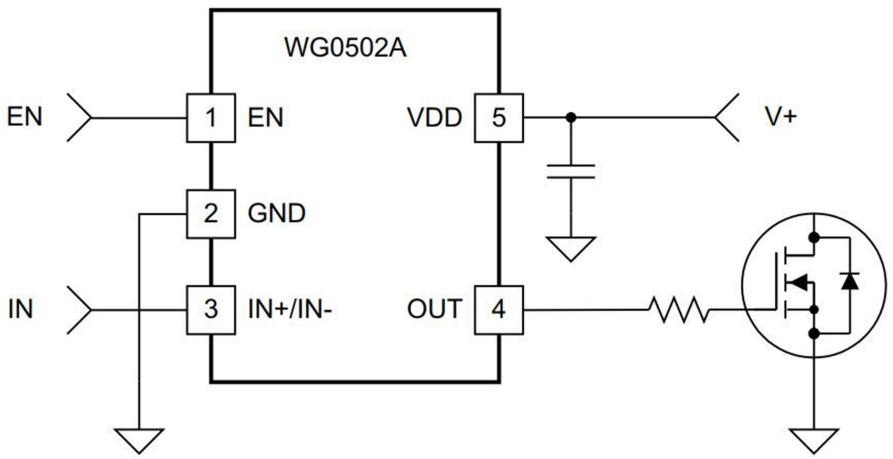
The WG0502A provide 5A source, 5A sink peak-drive current capability at V_{DD}=12V.The WG0502A is designed to operate over a wide V_{DD} range of 4.5V to 18V. Internal Under Voltage Lockout (UVLO) circuitry on V_{DD} pin holds output low outside V_{DD} operating range.

The capability to operate at low voltage levels such as below 5V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power semiconductor devices.

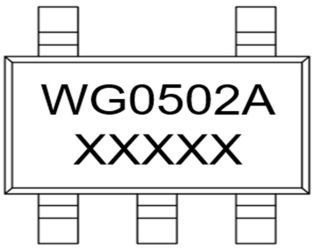
Applications

- Switch-Mode Power Supplies
- DC-DC Converters
- Companion Gate Driver Devices for Digital Power Controllers
- Solar Power, Motor Control, UPS
- Gate Driver for Emerging Wide Band-Gap Power Devices such as GaN

Typical Application Circuit

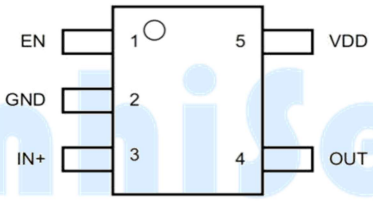


Ordering and Marking Information

Part Number	Marking Code	package
WG0502A	 WG0502A=Device code XXXXX= Special code	SOT23-5L

Pin configuration

SOT23-5L (TOP VIEW)



Pin Description

Pin No.	Name	Pin Function
1	EN	EN biased Low disables output regardless of Input state, EN biased high or floating enables output, EN is allowed to float.
2	GND	IC Ground Pin.
3	IN+	Non-inverting input in the WG0502A, output held Low if IN+ is unbiased or floating.
4	OUT	Sourcing and sinking current output of driver.The output driver for driving the external MOSFET.
5	VDD	Power supply input.

Device Functional Modes

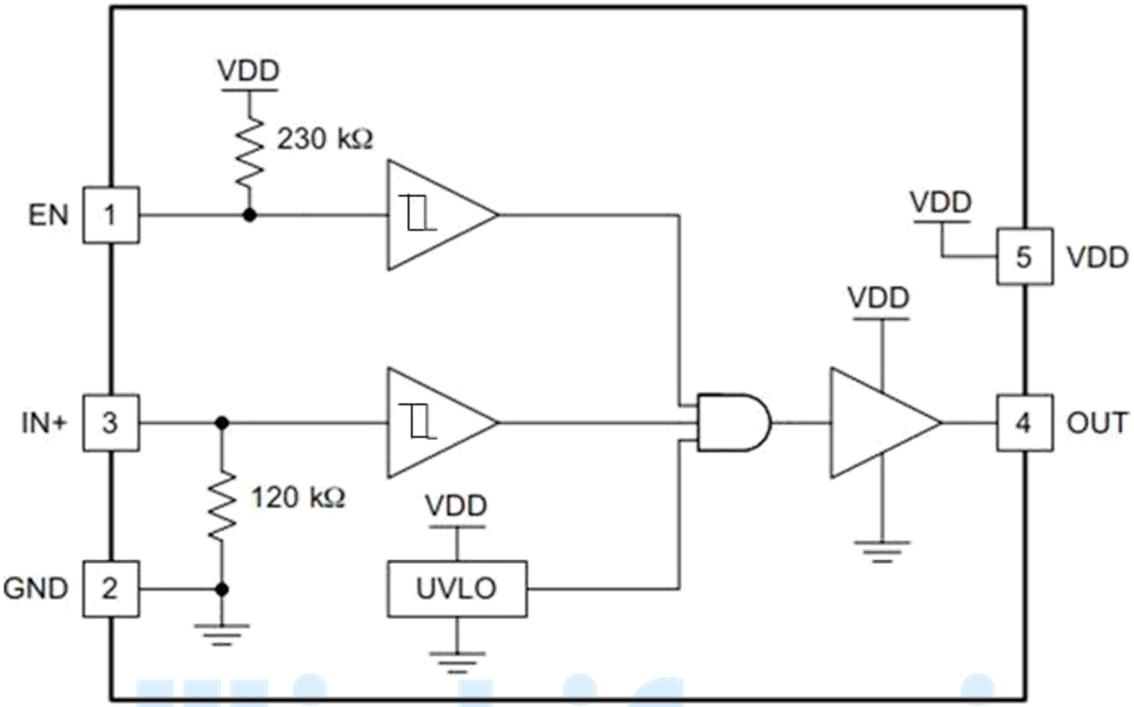
EN	WG0502A	
	INPUT PIN	OUT PIN
H	L	L
H	H	H
L	Any	L
Any	x	L
x	L	L
x	H	H

(1) x = Floating Condition

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage(VDD)	VDD	-0.3 to 20.0	V
OUT Voltage	OUT	-0.3 to VDD+0.3	V
Output Current(pulsed)		4	A
Output Current(continuous)		0.3	A
IN,EN Voltage	IN, EN	-0.3 to 20	V
ESD Human Body Rating		±2.0	KV
ESD,Charged Device Rating		±500	V
Lead Temperature(soldering,10sec)		230	℃
Junction Temperature		150	℃
Storage Temperature		-65 to 150	℃

Block Diagram



Electrical Characteristics (V_{DD} = 12.0V, 1uF capacitor from V_{DD} to GND.)

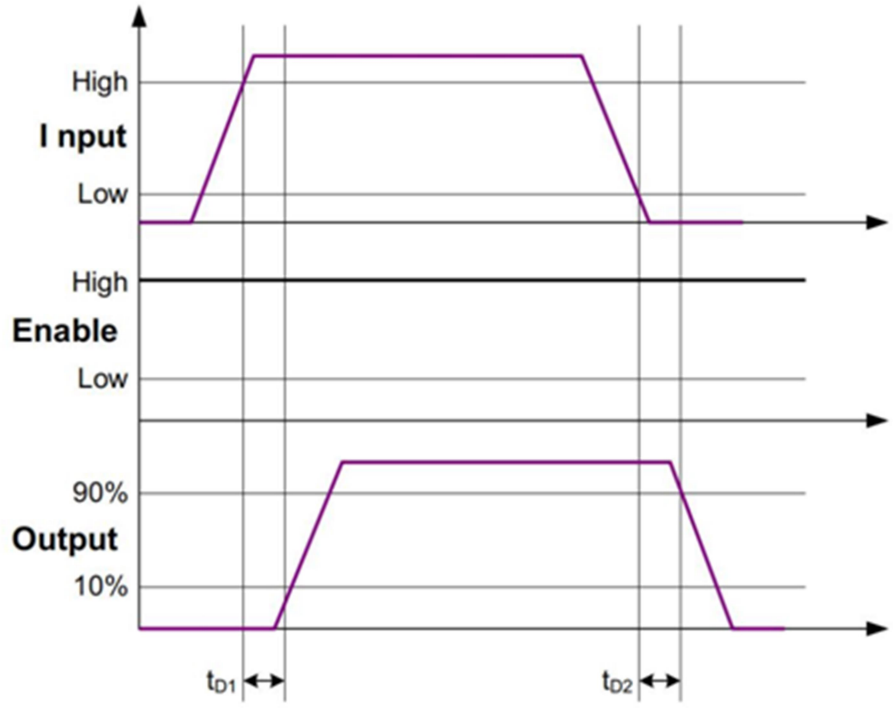
Parameter	Symbol	Condition		Min	Typ	Max	Unit
BIAS Currents							
Startup current	$I_{DD(off)}$	V_{DD}= 3.4 V	IN+ = V_{DD}	25	55	110	μA
			IN+ = Gnd	15	30	65	
Under Voltage Lockout (UVLO)							
Supply start threshold	V_{ON}	T_A = 25°C		3.85	4.20	4.57	V
		T_A = -40°C to 140°C		3.80	4.20	4.67	
Minimum operating voltage after supply start	V_{OFF}			3.45	3.9	4.35	
Supply voltage hysteresis	V_{DD_H}				0.3		
INPUTS							
Input signal high threshold	V_{IN_H}	V_{DD} = 12 V		1.9	2.1	2.3	V
Input signal low threshold	V_{IN_L}			0.9	1.2	1.4	
Input signal hysteresis	V_{IN_HYS}				0.9		
ENABLE (EN)							
Enable signal high threshold	V_{EN_H}	V_{DD} = 12 V		1.9	2.1	2.3	V
Enable signal low threshold	V_{EN_L}			0.9	1.2	1.3	
Enable hysteresis	V_{EN_HYS}				0.9		

Switching Characteristics V_{DD}=12V, over operating free-air temperature range

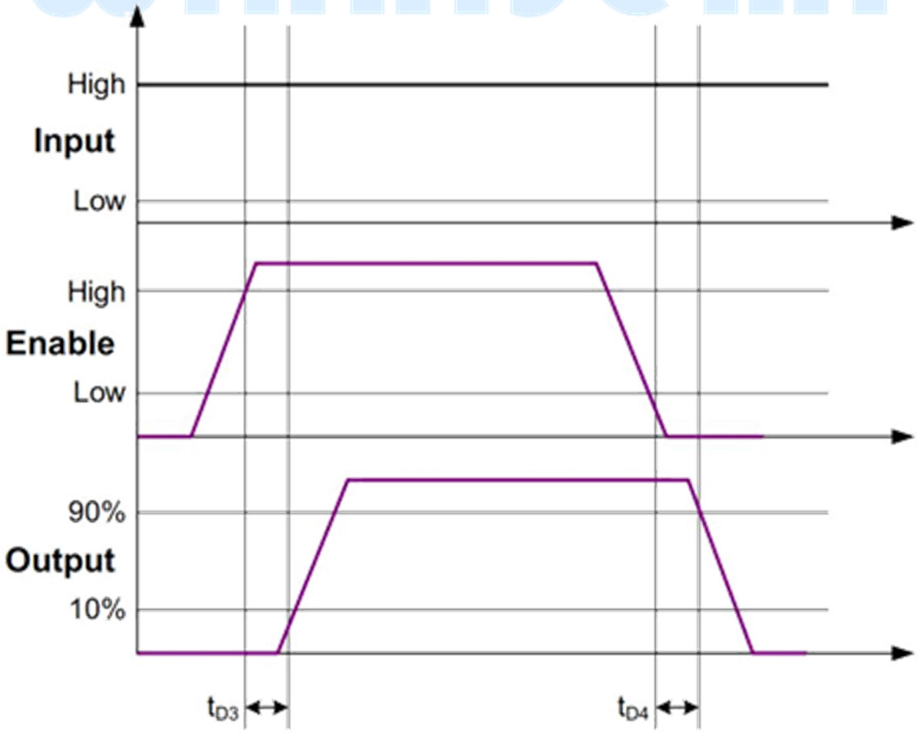
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Source/Sink Current						
Source,sink peak current	$I_{SRC/SNK}$	C_{LOAD} = 0.22 μF,F_{SW} = 1kHz		-5/+5		A
Outputs						
High output voltage	V_{DD} -V_{OH}	V_{DD} = 12 V I_{OUT} = -10mA		25		mV
Low output voltage	V_{OL}	V_{DD} = 12V I_{OUT} = 10mA		5		
Output pull-up resistance	R_{OH}	V_{DD} = 12V I_{OUT} = -10mA		2.5		Ω
Output pull-down resistance	R_{OL}	V_{DD} = 12V I_{OUT} = 10mA		0.5		

Switching Characteristics (V_{DD}=12V, over operating free-air temperature range)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Rise time	t_R	C_{LOAD}= 1.8nF		6		
Fall time	t_F	C_{LOAD}= 1.8nF		6		
Delay matching between 2 channels	t_M	INA=INB, OUTA=OUTB at 50% transition point		1		
Minimum input pulse width that changes the output state	t_{PW}			15		
Input to output propagation delay	t_{D1}	C_{LOAD}= 1.8nF, 5V input pulse		9		
	t_{D2}	C_{LOAD}= 1.8nF, 5V input pulse		9		
EN to output propagation delay	t_{D3}	C_{LOAD}= 1.8nF, 5V enable pulse		9		
	t_{D4}	C_{LOAD}= 1.8nF, 5V enable pulse		9		



Non-inverting Configuration



Enable and Disable Function

Typical Performance Characteristics

Fig.1 Operating Supply Current vs Frequency

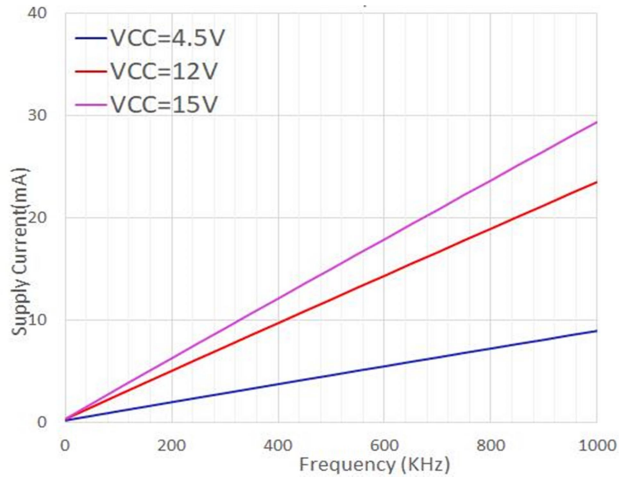


Fig.2 Propagation Delay vs Supply Voltage

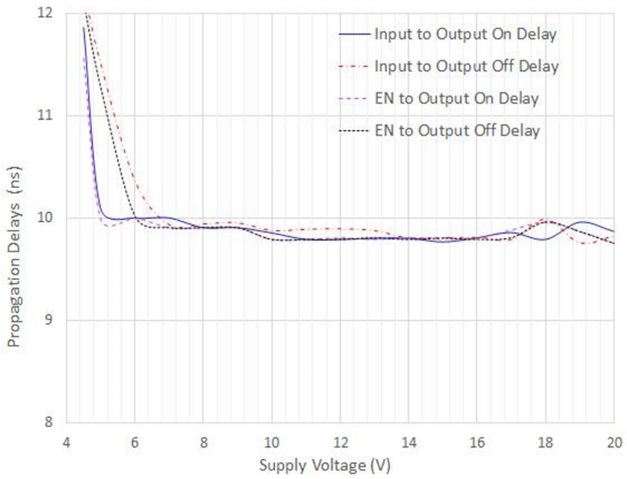


Fig.3 Rise Time vs Supply Voltage

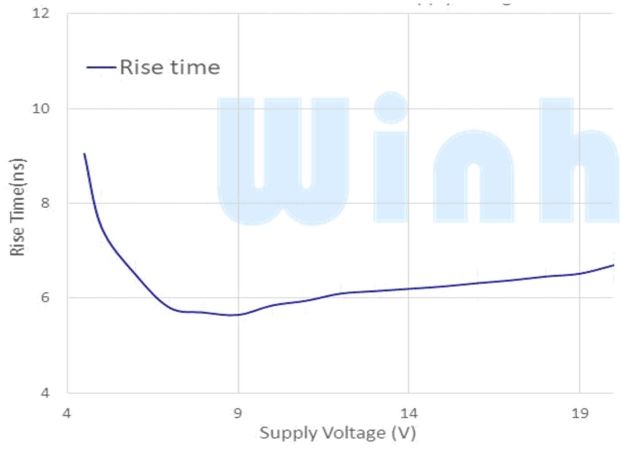


Fig.4 Fall Time vs Supply Voltage

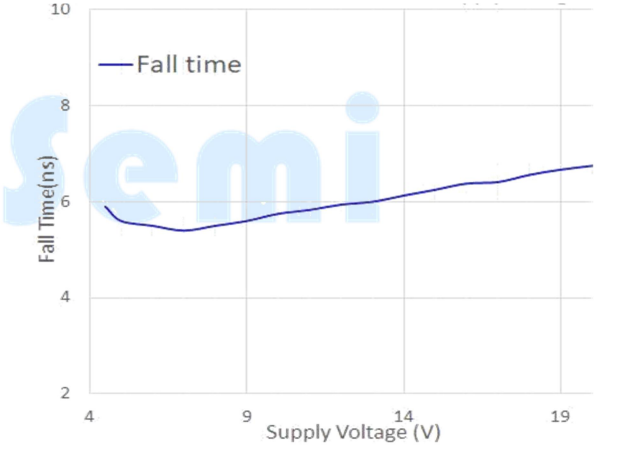


Fig.5 Start-Up Current vs Temperature

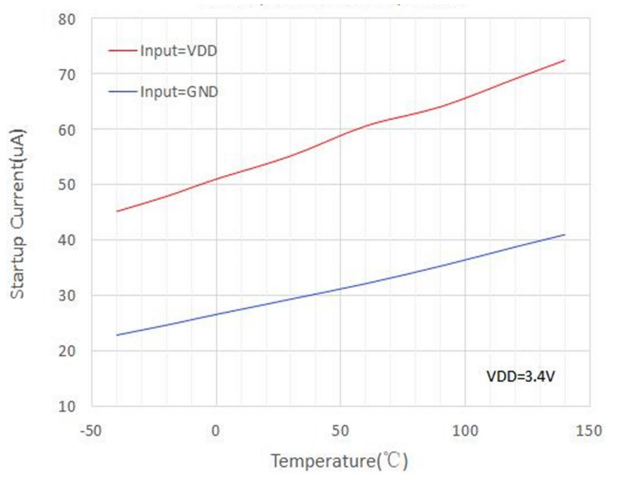


Fig.6 Operating Supply Current vs Temperature (Output Switching)

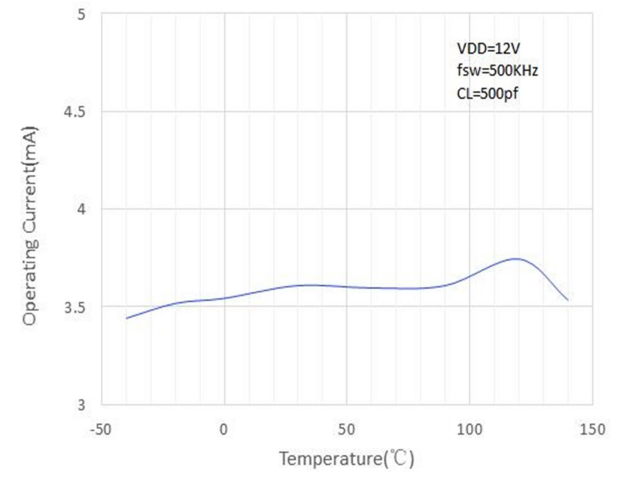


Fig.7 Operating Supply Current vs Temperature(Output in DC On/Off Condition)

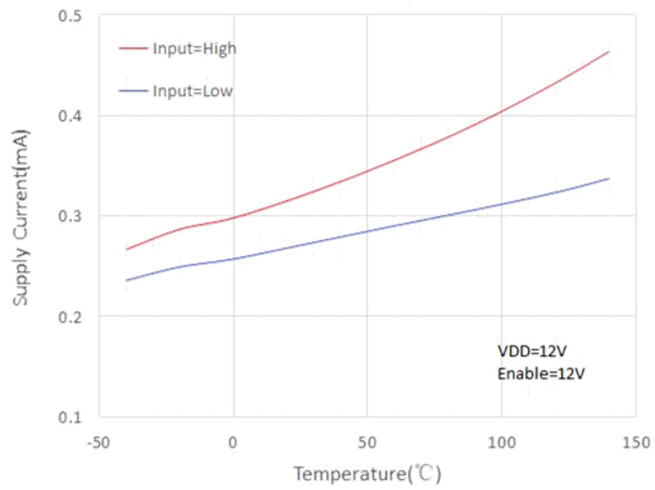


Fig.8 UVLO Threshold vs Temperature

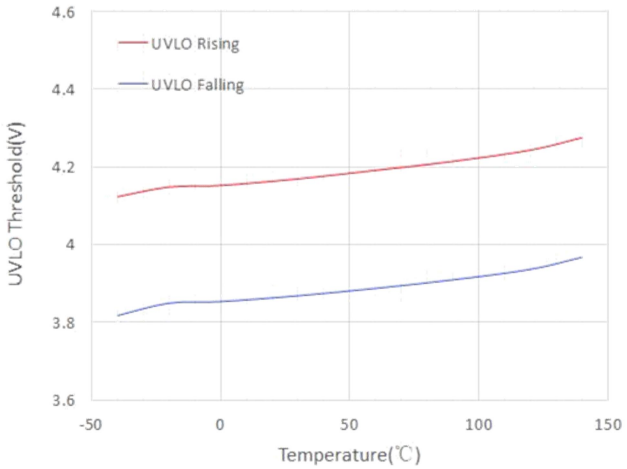


Fig.9 Input Threshold vs Temperature

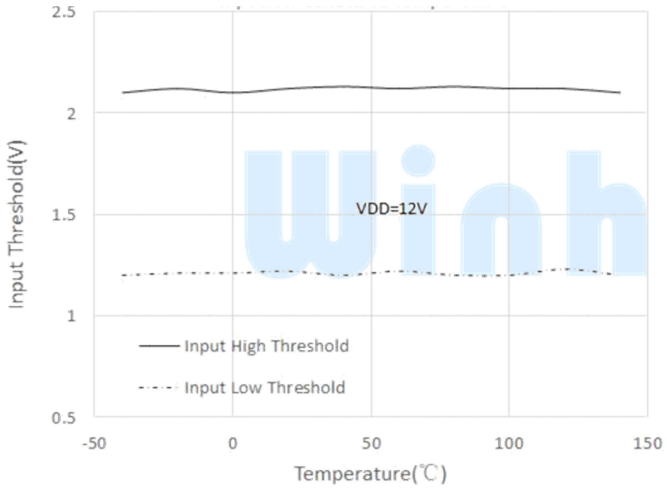


Fig.10 Rise Time vs Temperature

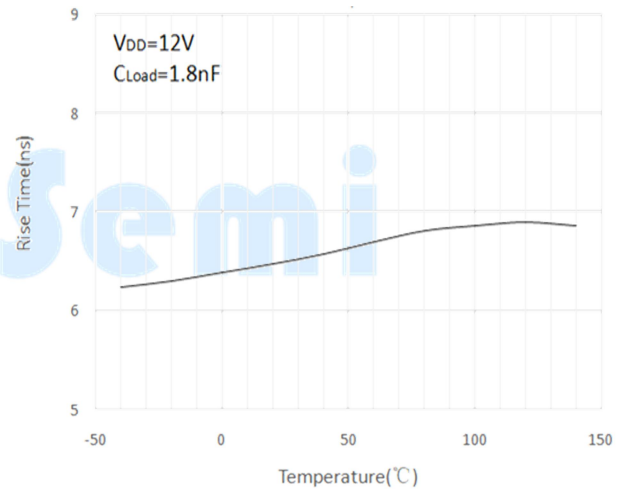


Fig.11 Fall Time vs Temperature

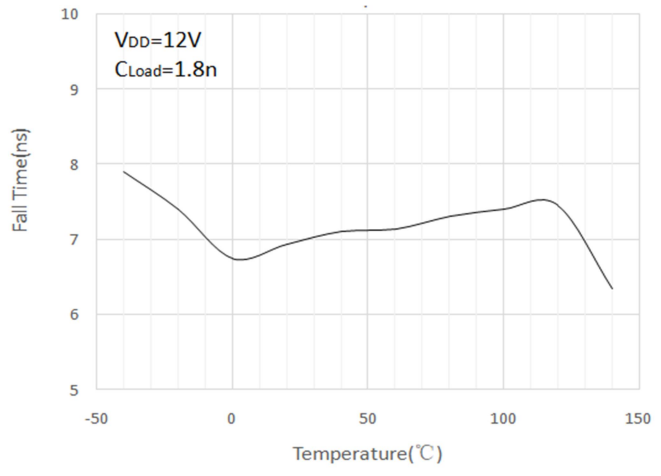


Fig.12 Input to Output Propagation Delay vs Temperature

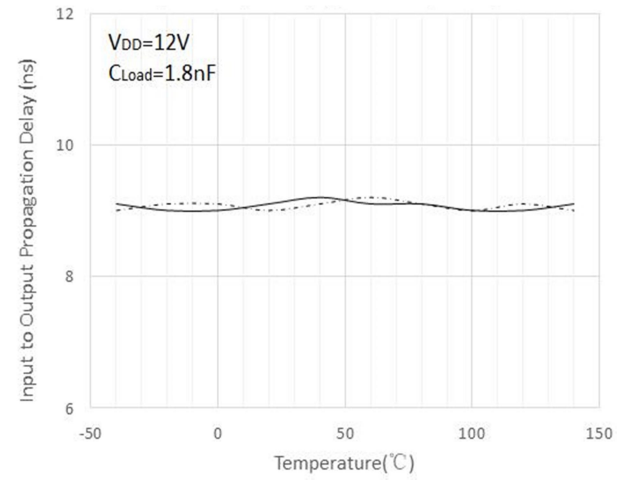


Fig.13 Output Pull up Resistance vs Temperature

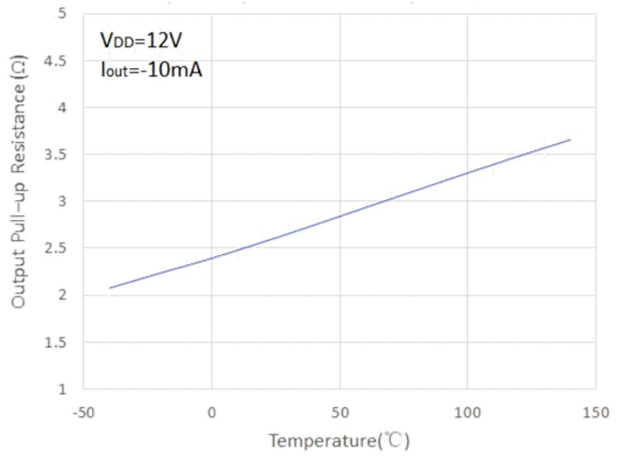


Fig.14 Output Pull Down Resistance vs Temperature

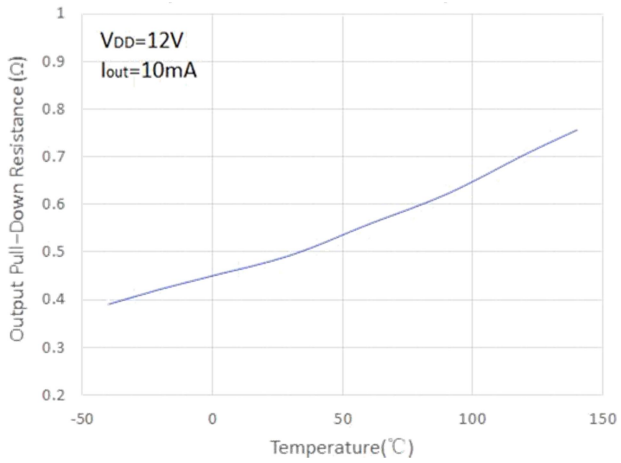
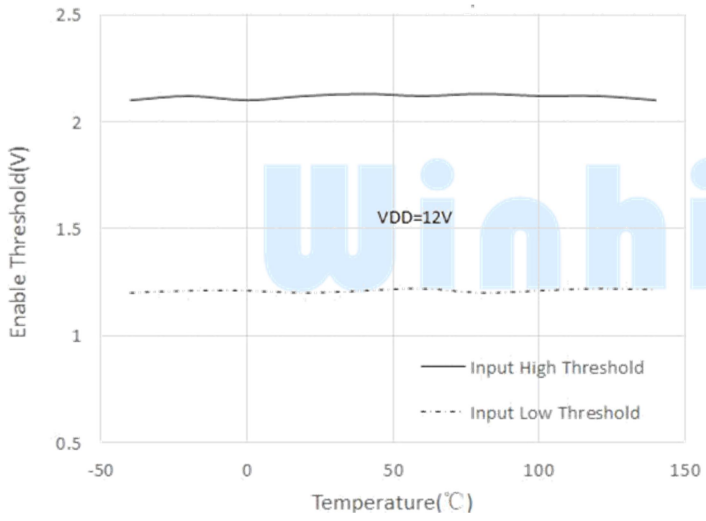


Fig.15 Enable Threshold vs Temperature



Applications Information

Introduction

The WG0502A single-channel, high-speed, low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the WG0502A device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 9ns .

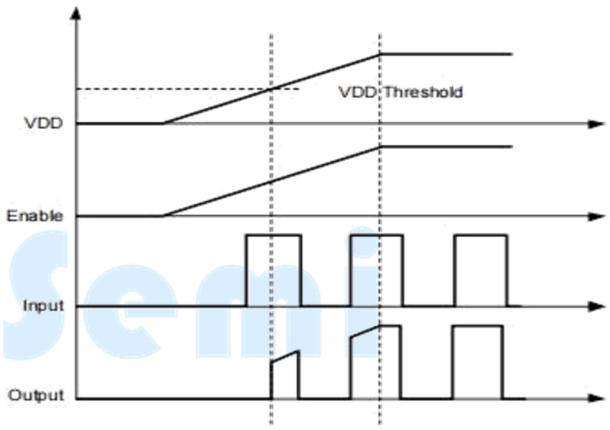
Supply Voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability ofWG0502A when driving very large MOSFETs. The minimum operating supply voltage is set by the under voltage lockout function to a typical default value of 4.2 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

The WG0502A device provides 5A source, 5A sink peak-drive current capability. The bias supply voltage range for which the WG0502A device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal under voltage-lock out protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the V_{DD} pin of the device. Keeping a 2V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V. It is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

Under voltage Lockout (UVLO)

The Under voltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 4.2V(with hysteresis). UVLO of 4.2 V is normally used for logic level based MOSFETs.



Power-up in a Non-Inverting Driver Channel

The WG0502A device follows non-inverting logic. The input pins of the devices are based on what is known as CMOS input threshold logic. In CMOS input logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. This offers the benefits of higher noise immunity due to the higher threshold voltage , as well as the ability to accept slow dv/dt input signals for manipulating the propagation delay between the PWM controller signal and the gate driver output. For system robustness, internal pull-up and pull-down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition.

Driver Outputs

In order to effect fast switching of power devices and reduce associated switching power losses, a powerful

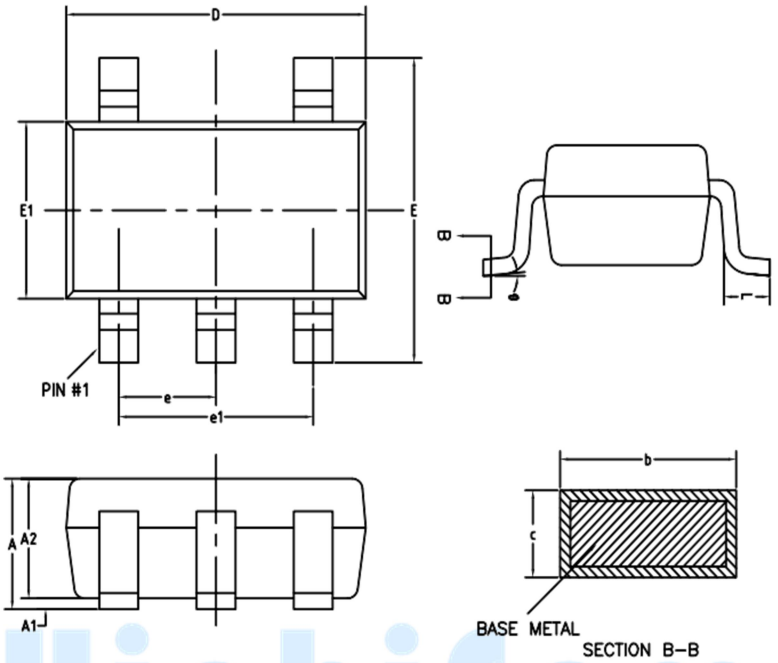
gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. High-current gate driver devices are required in switching power applications for a variety of reasons. Emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low V_{DD} voltages, low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design. The WG0502A device provides 5A source, 5A sink peak-drive current capability. The device is designed to operate over a wide V_{DD} range of 4.5 to 18V. Internal under voltage lockout circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The bias supply voltage range for which the WG0502A device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal under voltage-lockout protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition with the V_{DD} pin voltage below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the V_{DD} pin of the device. Keeping a 2V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V. The UVLO protection feature also involves a hysteresis function. When the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, if the voltage drops, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification V_{DD_H}.

While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_{OFF} threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the V_{ON} threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. The charge for source current pulses delivered by the out pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin , a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V_{DD} and Gnd pins and located as close to the device as possible, for the purpose of decoupling.

Mechanical Dimensions

Package Information SOT23-5L



SYMBOL	MILLIMETER	
	MIN	MAX
A	0.9	1.45
A1	0	0.15
A2	0.9	1.3
b	0.28	0.5
c	0.1	0.23
D	2.82	3.05
E	2.6	3
E1	1.5	1.75
e	0.95BSC	
e1	1.8	2
L	0.3	0.6
θ	0°	8°

Note:

1. Followed from JEDEC MO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 10mil per si.

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