



VFN080N10TA1

Datasheet

Description

Low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low V_{th} series is specially optimized for synchronous rectification systems with low driving voltage.

Applications

- Switching voltage regulator
- PD charger
- Motor driver
- DC-DC convertor
- Switched mode power supply

Features

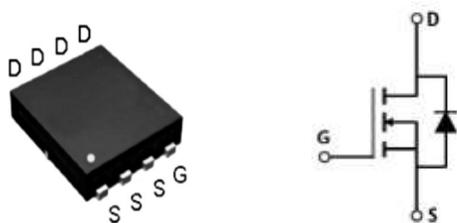
- Low $R_{DS(ON)}$ and FOM
- Extremely Low Switching Loss
- Excellent Reliability and Stability
- Fast switching and soft recovery

Key Performance Parameters

Parameter	Value	Unit
$V_{DS,min} @ T_{j,max}$	100	V
$R_{DS(on),max} @ V_{GS}=10V$	8	mΩ
Q_g	33.9	nC
$I_{D,pulse}$	210	A

Packaging and Internal Circuit

Part Name	Package	Marking
VFN080N10TA1	PDFN5*6	VFN080N10TA1



Absolute Maximum Ratings (T_j=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source voltage	V _{DS}	100	V
Gate-source voltage	V _{GS}	±20	V
Continuous drain current ¹⁾ , T _C =25°C	I _D	70	A
Pulsed drain current ²⁾ , T _C =25 °C	I _D , pulse	210	A
Continuous diode forward current ¹⁾ , T _C =25 °C	I _S	70	A
Diode pulsed current ²⁾ , T _C =25 °C	I _S , pulse	210	A
Power dissipation ³⁾ , T _C =25 °C	P _D	100	W
Single pulsed avalanche energy ⁵⁾	E _{AS}	45	mJ
Operation and storage junction temperature	T _{stg} , T _j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R _{θJC}	1.25	°C/W
Thermal resistance, junction-ambient ⁴⁾	R _{θJA}	62	°C/W

Static Characteristics (T_j=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Drain-source on-state resistance	R _{DSS(on)}	V _{GS} =10V, I _D =30A		6.3	8.0	mΩ
Drain-source on-state resistance	R _{DSS(on)}	V _{GS} =4.5V, I _D =12A		7.6	10	mΩ
Gate threshold voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	1.5		2.5	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-source leakage current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate resistance	R _G	f=1 MHz, Open drain		4		Ω

Dynamic Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=100kHz		2350		pF
Output capacitance	C _{oss}			1281		pF
Reverse transfer capacitance	C _{rss}			100		pF
Turn-on delay time	t _{d(on)}	V _{GS} =10V V _{DS} =50V, R _G =2Ω, I _D =25A		14.5		ns
Rise time	t _r			7.4		ns
Turn-off delay time	t _{d(off)}			40.2		ns
Fall time	t _f			17		ns

Gate Charge Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gate to source charge	Q _{gs}	V _{GS} =10V, V _{DS} =50V, I _D =25A		5.1		nC
Gate to drain charge	Q _{gd}			8.1		nC
Gate charge total	Q _g			33.9		nC
Gate plateau voltage	V _{plateau}			3.1		V

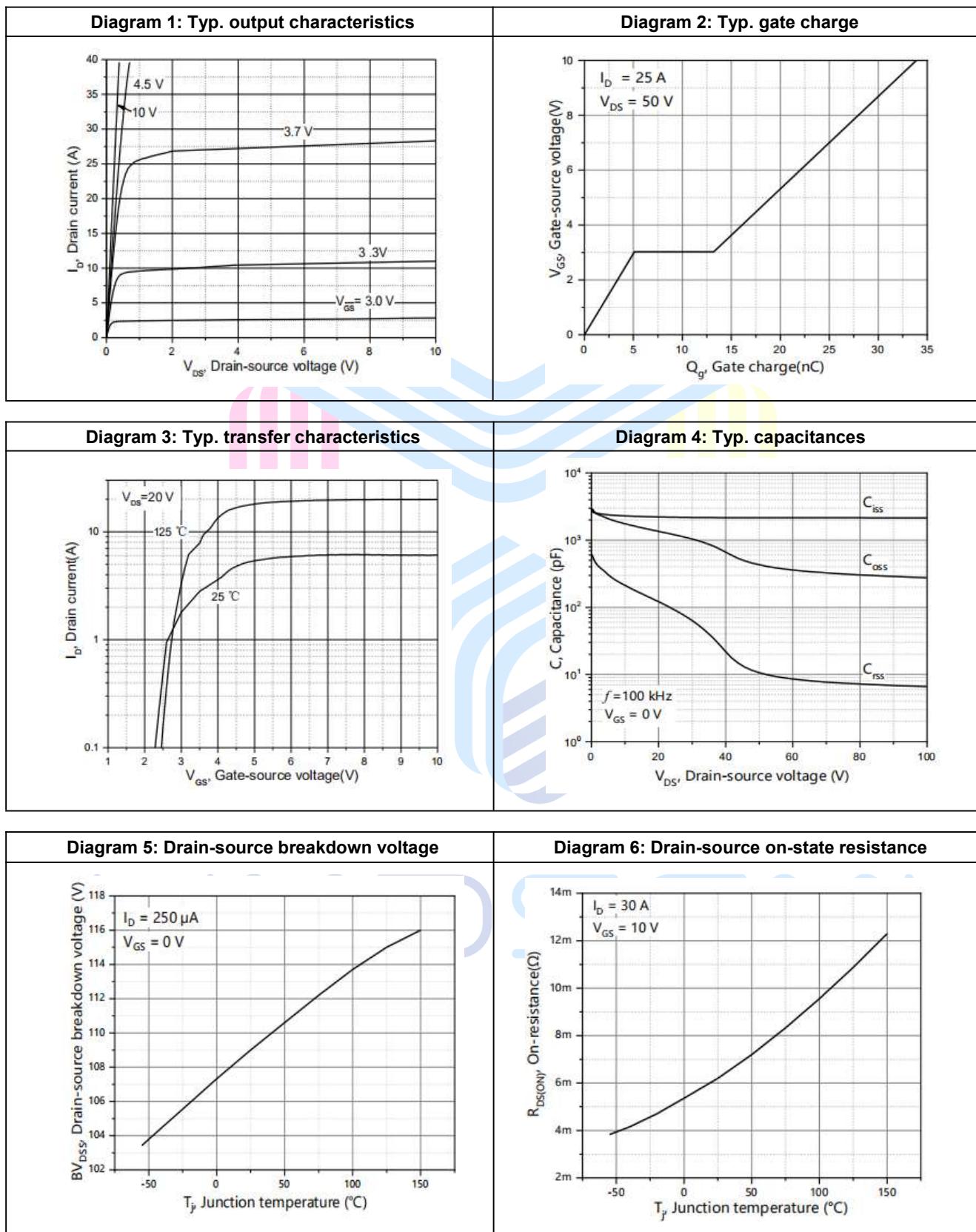
Body Diode Characteristics

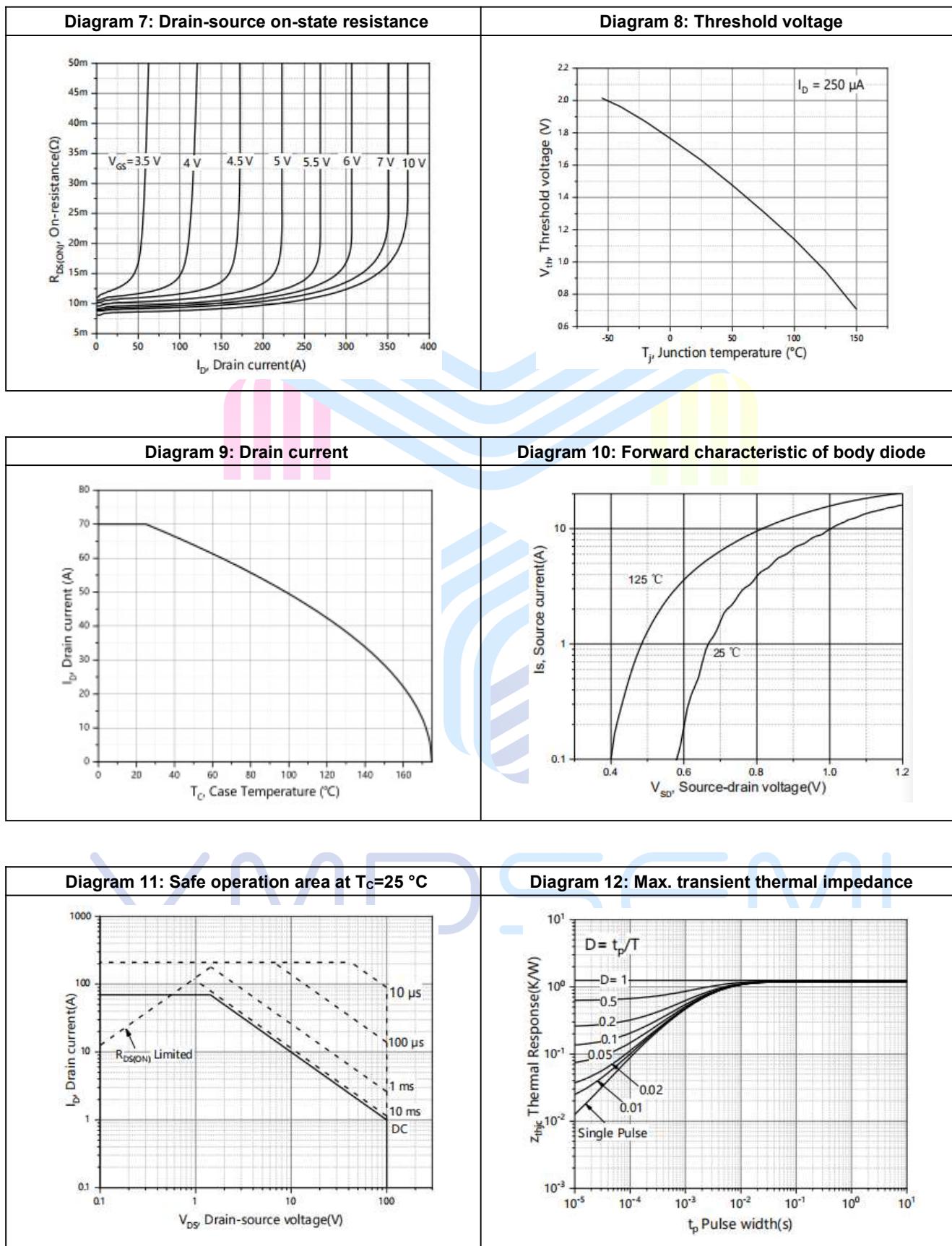
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Diode forward voltage	V _{SD}	V _{GS} =0V, I _S =20A			1.3	V
Reverse recovery time	t _{rr}	V _R =50V, I _S =25A, di/dt = 100A/μs		51.1		ns
Reverse recovery charge	Q _{rr}			102.3		nC
Peak reverse recovery current	I _{rrm}			2.9		A

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5) V_{DD}=50 V, V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical characteristics diagram





Test Circuits and waveforms

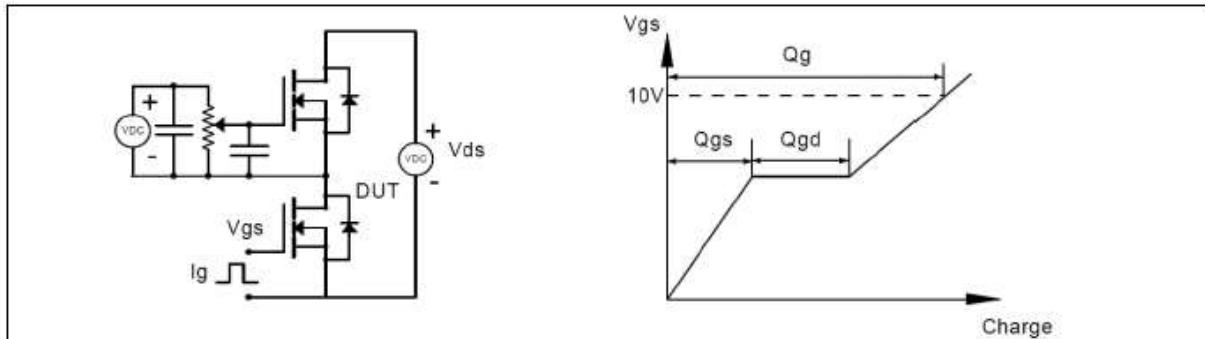


Figure 1. Gate charge test circuit & waveform

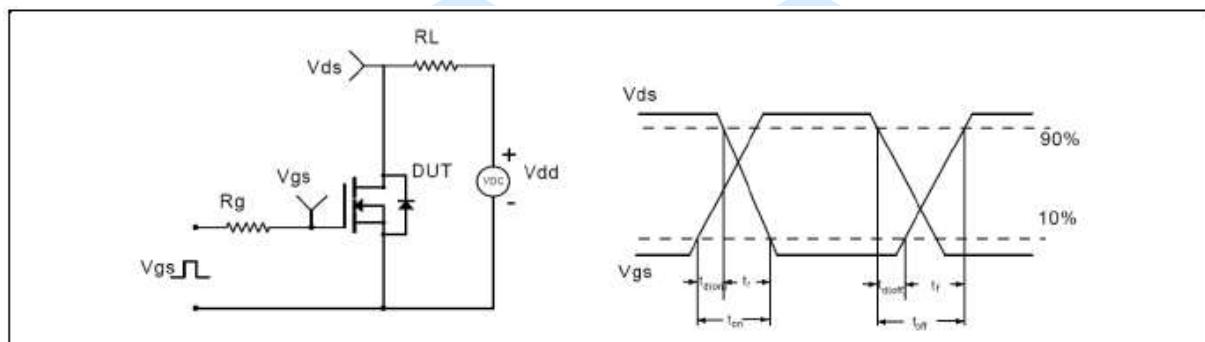


Figure 2. Switching time test circuit & waveforms

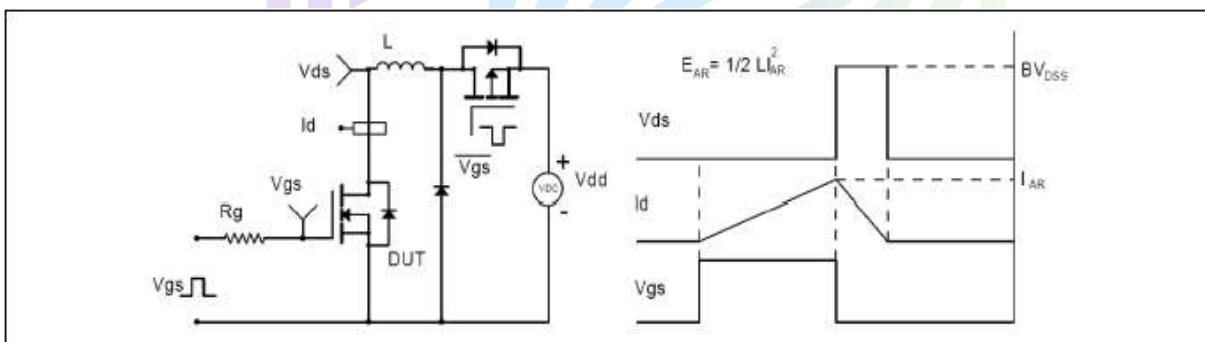


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

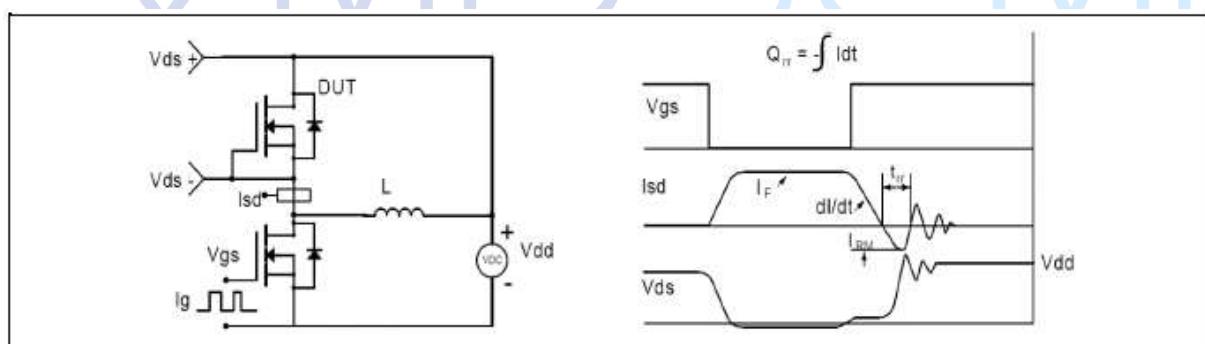
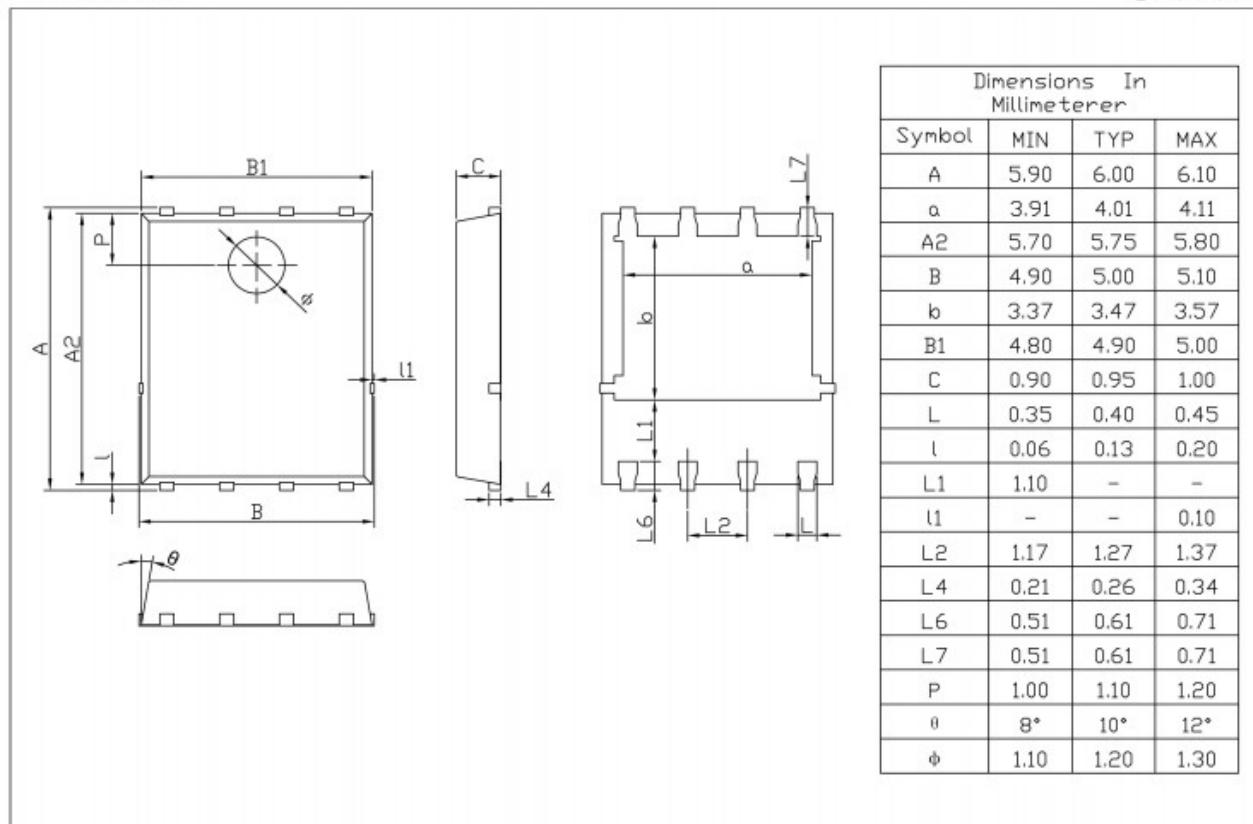


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outlines

PDFN5 X6

Unit:mm


Outline PDFN5*6


Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2021-05-08	Release version



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