VFPB010R095NA

Datasheet

General Description

The VMD VFPB010R095NA MOSFET is based on unique device design to achieve low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially optimized for high systems with gate driving voltage greater than 10V.

Symbol

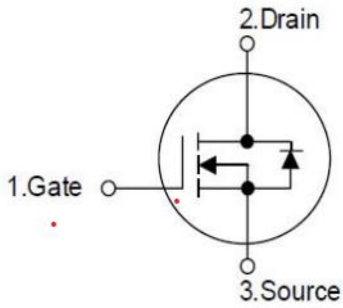
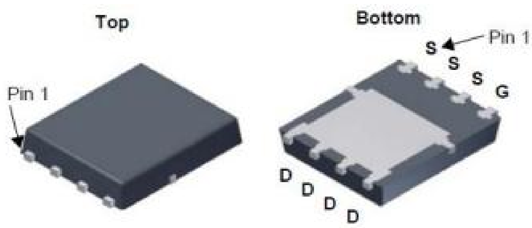


Figure 1 Symbol of VFPB010R095NA

Features

- Ultra Low $R_{DS(ON)\_max}$ = 9.5mΩ@V_{GS} = 10V.
- Extremely low switching loss
- Excellent stability and uniformity
- 100% UIS tested , 100% △VDS Tested
- RoHS and Halogen-Free Compliant

Package Type



DFN5*6

Figure 2 Package Type of VFPB010R095NA

Application

- Charger / Adapter
- Server/Telecom
- Synchronous Rectification
- High Frequency Switching

Ordering Information

Product Name	Package
VFPB010R095NA	PDFN5*6

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C=25ºC(Note 5)	I_D	60	A
	T_C=100ºC(Note 5)		38	
Pulsed Drain Current (Note 3)		I_{DM}	240	A
Power Dissipation,T_C=25ºC(Note 2)		P_D	63	W
Avalanche Energy, Single Pulse (Note 3,Note6)		E_{AS}	90	mJ
Avalanche Current, Repetitive (Note 3,Note6)		I_{AS}	19	A
Operating and Storage Temperature Range		T_J,T_{STG}	-55 to 150	ºC

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			2.0	ºC/W
Thermal Resistance, Junction-to-Ambient(Note 1,Note4)	$R_{\theta JA}$			55	ºC/W

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with TA =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
2. The power dissipation PD is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is V_{DS}=50V,V_{GS}=10V,L=0.5mH

Electrical Characteristics T_J= 25 ºC, unless otherwise specified

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	1.2	1.8	2.6	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		8.2	9.5	mΩ
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=4.5V, I_D=10A		11.3	13.5	mΩ
Forward Threshold Voltage		g_{fs}	V_{DS}= 5V, ID= 20A		13.5		S
Gate Resistance		R_G	F=1MHz, Open Drain		1.94		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=50, V_{GS}=0V, f=1MHz		2122		pF
Output Capacitance		C_{OSS}			618		
Reverse Transfer Capacitance		C_{RSS}			25		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=50V, I_D=20A, R_G=3.0Ω, V_{GS}=10V		17		ns
Rise Time		t_r			4		
Turn-off Delay Time		$t_{d(off)}$			32		
Fall Time		t_f			8		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=50V, I_D=20A, V_{GS}=10V		9		nC
Gate to Drain Charge		Q_{gd}			10		
Gate Charge Total		Q_g			41.8		
Reverse Diode Characteristics							
Continuous Source Current		I_s				60	A
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=20A		0.88	1.0	V
Reverse Recovery Time		t_{rr}	I_{SD}=20A, dI_F/dt=100A/us		50.5		ns
Reverse Recovery Charge		Q_{rr}			71.5		nC

Typical Performance Characteristics

Figure 3: Maximum Power Dissipation vs Case Temperature

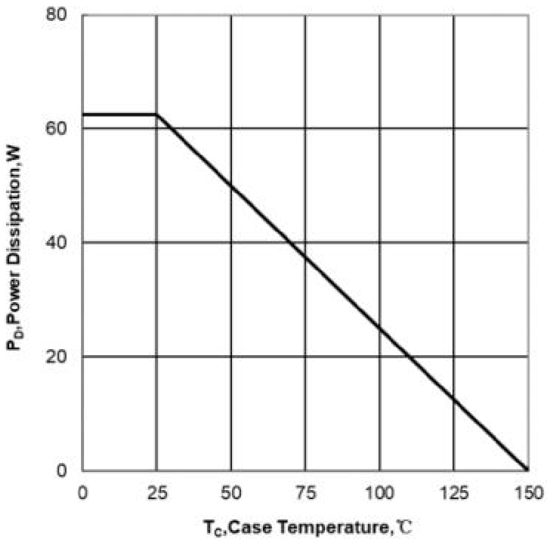


Figure 4: Gate Charge

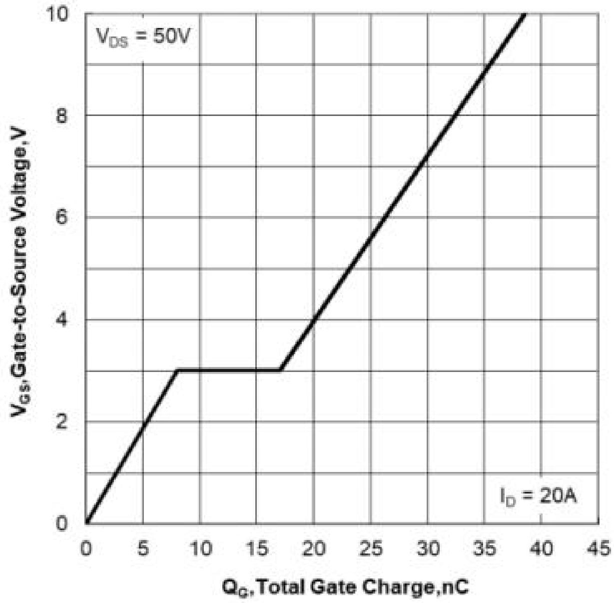


Figure 5: Maximum Continuous Drain Current vs Case Temperature

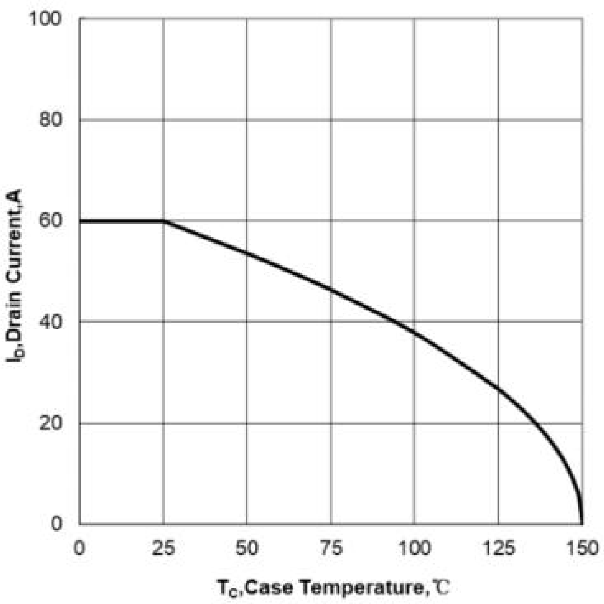


Figure 6: Output Characteristics

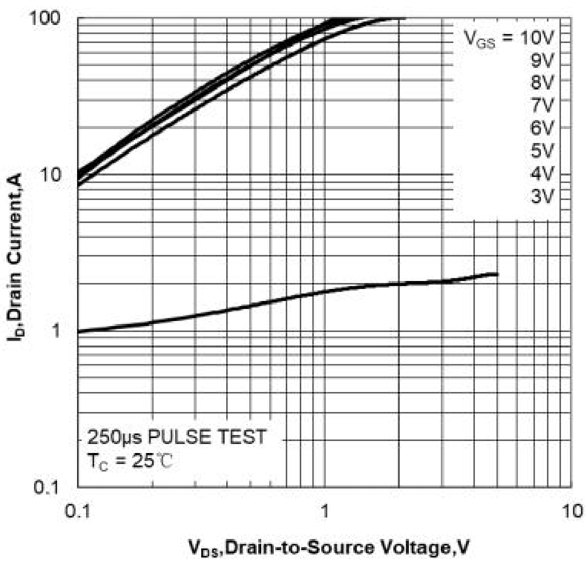


Figure 7: Drain-to-Source On Resistance vs Drain Current

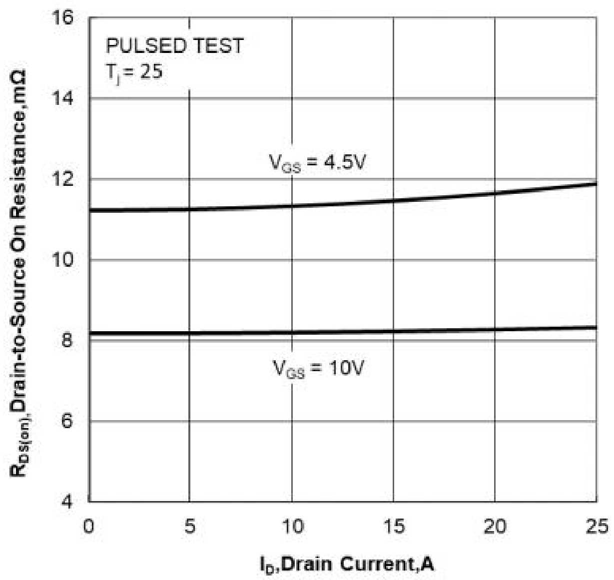


Figure 8: Transfer Characteristics

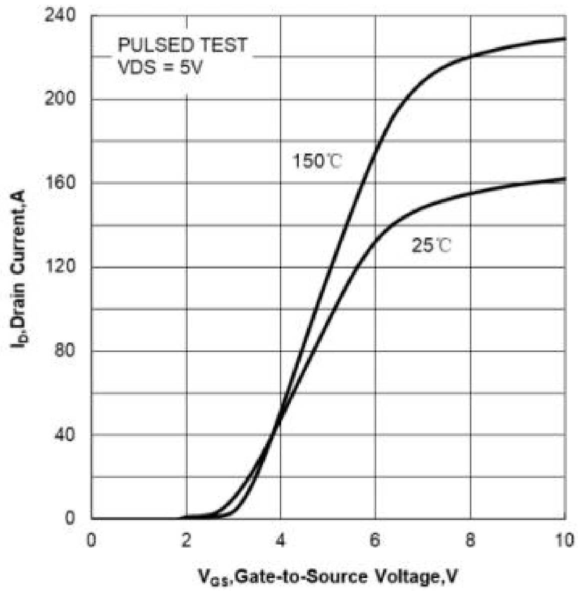


Figure 9: Body Diode Forward Voltage vs Source Current and Temperature

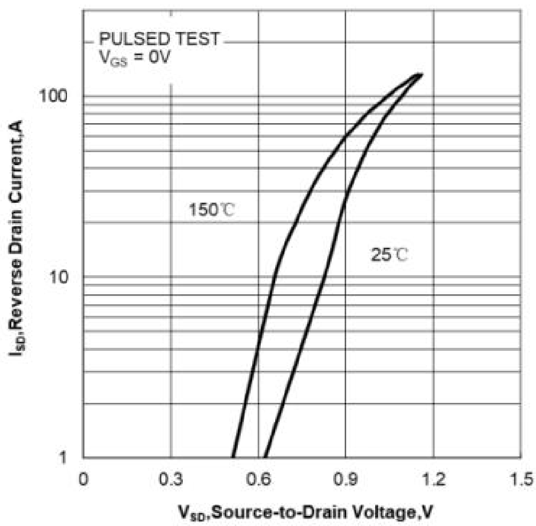


Figure 10: Capacitance Characteristics

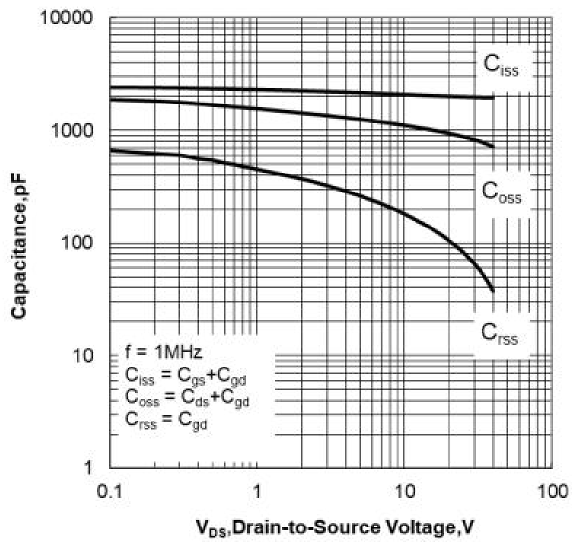


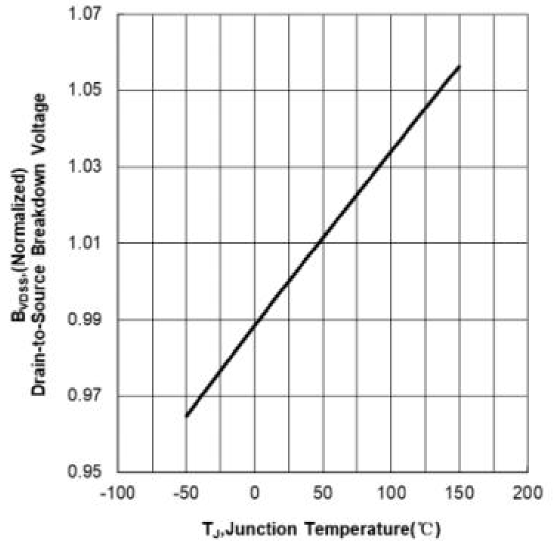
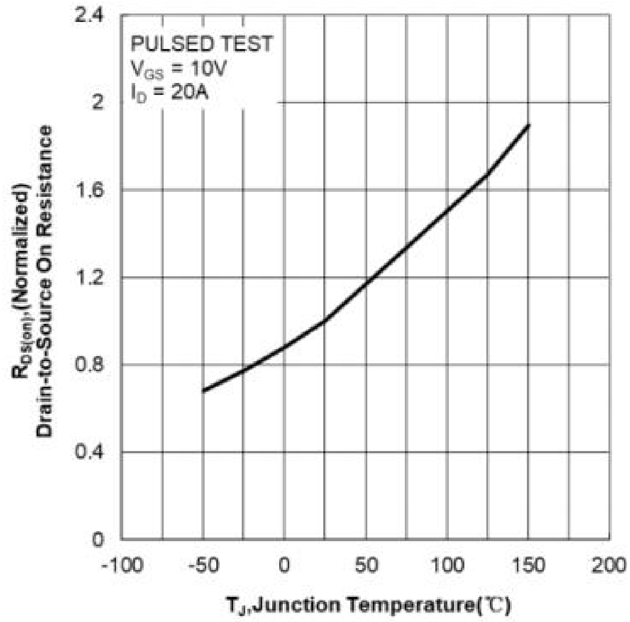
Figure 11: Normalized Breakdown Voltage vs Junction Temperature	Figure 12: Normalized On Resistance vs Junction Temperature
	

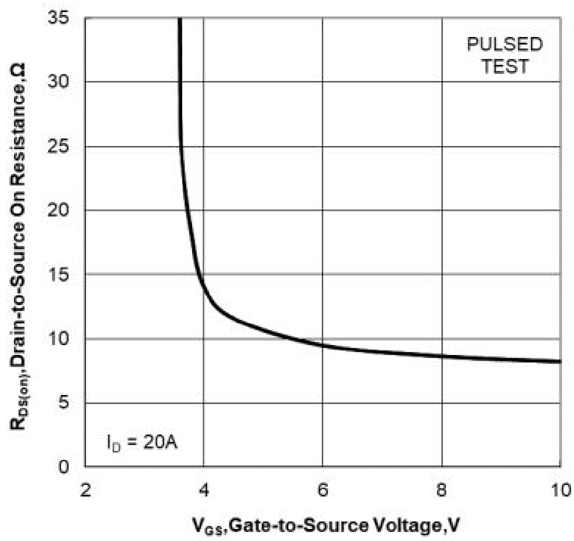
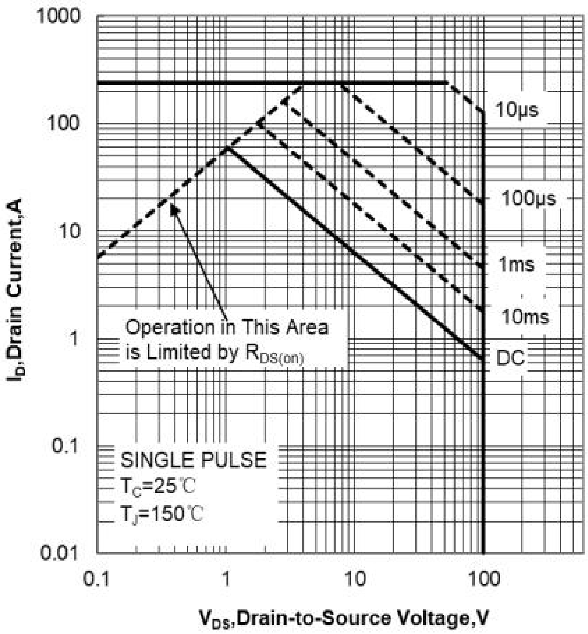
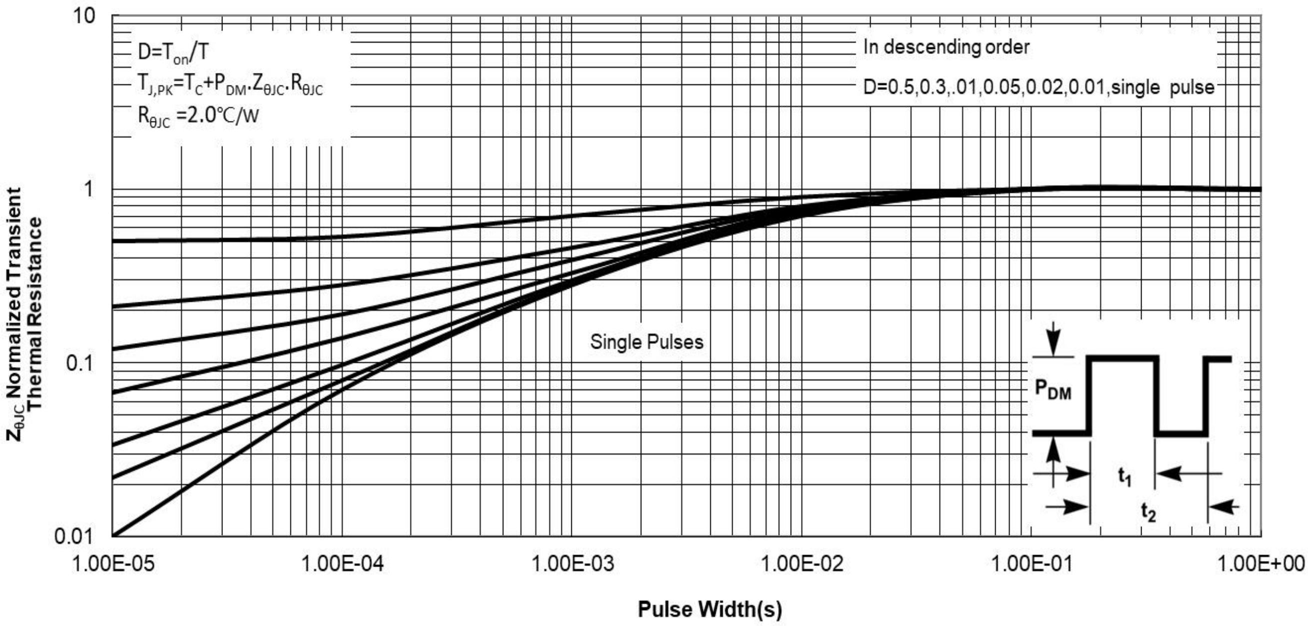
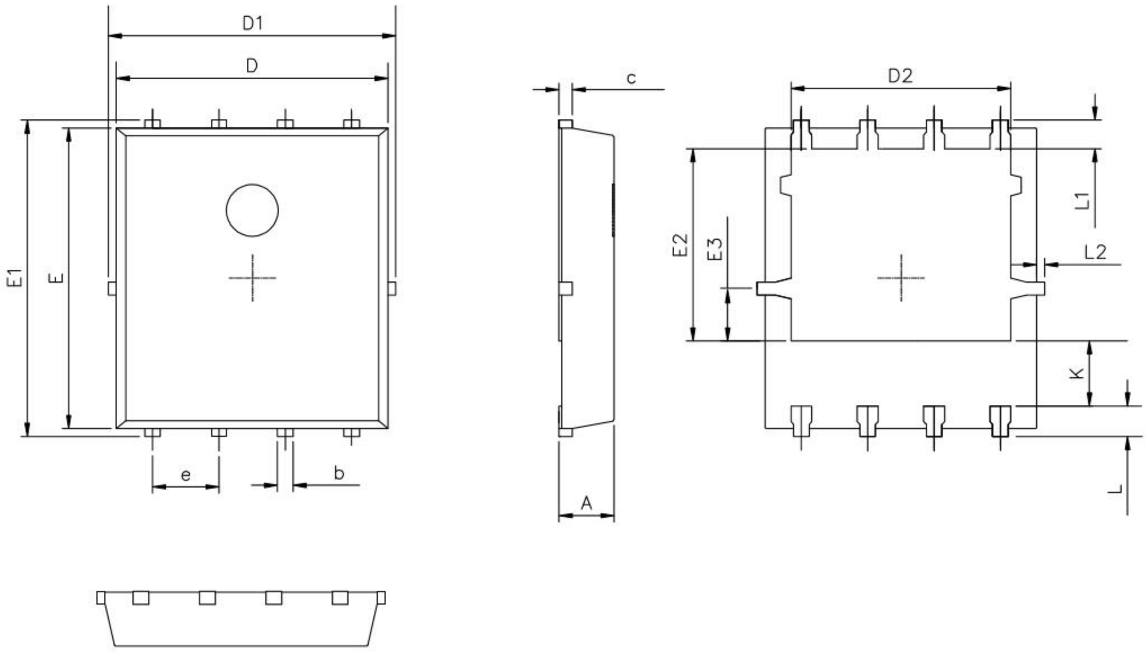
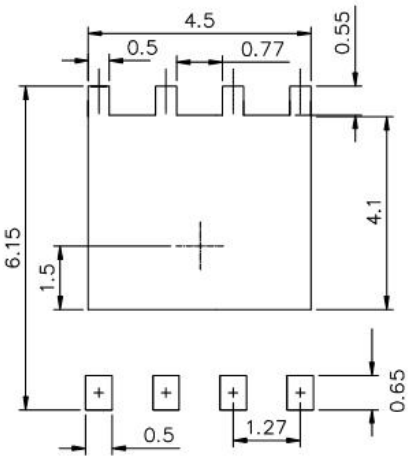
Figure 13: Drain-to-Source On Resistance vs Gate Voltage and Drain Current	Figure 14: Maximum Safe Operation Area
	

Figure 15: Max, Transient Thermal Impedance



Mechanical Dimensions （PDF5*6 Unit: mm）





Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.9	1.0	1.10
b	0.25	0.35	0.50
c	0.10	0.20	0.30
D	4.80	5.00	5.30
D1	4.90	5.10	5.50
D2	3.92	4.02	4.20
E	5.65	5.75	5.85
E1	5.90	6.05	6.20
E2	3.325	3.525	3.775
E3	0.80	0.90	1.00
e		1.27	
L	0.40	0.55	0.70
L1		0.65	
L2	0.00		0.15
K	1.00	1.30	1.50

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