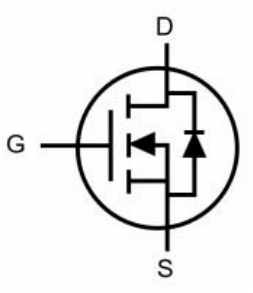
# VFTA020R130NA

# Datasheet

## General Description

| $V_{(BR)DSS}$ | $R_{DS(ON)\_max}$ | $I_D$ |
|---|---|---|
| 200V | 13mΩ@10V | 150A |

## Symbol

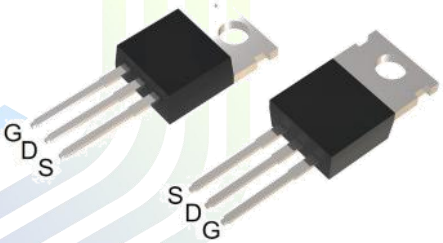



Symbol of VFTA020R130NA

## Features

- Low $R_{DS(ON)}$
- 100% Avalanche Tested
- 100% Rg Tested
- Enhancement mode
- Fast switching and High efficiency

## Package Type




TO-220

Package Type of VFTA020R130NA

## Application

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC converter
- Switched mode power supply

## Ordering Information

| Product Name | Package |
|---|---|
| VFTA020R130NA | TO-220 |

## Absolute Maximum Ratings ($T_A$= 25 ºC, unless otherwise specified)

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 200 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current (Silicon limited) | $T_C$=25ºC | $I_D$ | 150 | A |
| Continuous Drain Current (Silicon limited) | $T_C$=100ºC | | 106 | |
| Pulsed Drain Current Note 1 | $T_C$=25ºC | $I_{D.pulse}$ | 400 | A |
| Diode Forward Current | $T_C$=25ºC | $I_S$ | 150 | A |
| Continuous Drain Current | $T_A$=25ºC | $I_{DSM}$ | 8 | A |
| Continuous Drain Current | $T_A$=70ºC | | 6 | A |
| Max Power Dissipation Note3 | $T_C$=25ºC | $P_D$ | 750 | W |
| Max Power Dissipation Note4 | $T_A$=25ºC | $P_{DSM}$ | 2.1 | W |
| Avalanche Energy, Single Pulse Note 2 | | $E_{AS}$ | 1296 | mJ |
| Operation and storage temperature | | $T_J$,$T_{STG}$ | -55 to 175 | ºC |

## Thermal Resistance

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Thermal Resistance, Junction-to-Case Note5 | $R_{θJC}$ | - | 0.17 | 0.2 | ºC/W |
| Thermal Resistance, Junction-to-Ambient Note6 | $R_{θJA}$ | - | 50 | 60 | |

## Electrical Characteristics($T_J$= 25 ºC, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Statistic Characteristics** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250uA | 200 | - | - | V |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | $V_{DS}$=200V, $V_{GS}$=0V | - | - | 1 | uA |
| Zero Gate Voltage Drain Current $T_J$= 125 ºC | | | $V_{DS}$=200V, $V_{GS}$=0V | - | - | 100 | uA |
| Gate-Body Leakage Current | Forward | $I_{GSSF}$ | $V_{GS}$=20V, $V_{DS}$=0V | - | - | 100 | nA |
| | Reverse | $I_{GSSR}$ | $V_{GS}$=-20V, $V_{DS}$=0V | - | - | -100 | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250uA | 2.6 | 3.1 | 3.6 | V |
| Drain-Source On-Resistance[Note8] | | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=50A | - | 10 | 13 | mΩ |
| Drain-Source On-Resistance[Note8] $T_J$= 100 ºC | | | | - | 13 | - | |
| Gate resistance | | $R_G$ | f=1 MHz, Open drain | - | 4.1 | - | Ω |
| **Dynamic Characteristics**[Note7] | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{DS}$=100V | - | 4650 | - | pF |
| Output Capacitance | | $C_{OSS}$ | $V_{GS}$=0V | - | 410 | - | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | f=1MHz | - | 20 | - | pF |
| Turn-on Delay Time | | $t_{d(on)}$ | $V_{DS}$=100V | - | 18 | - | ns |
| Rise Time | | $t_r$ | $I_D$=50A | - | 61 | - | |
| Turn-off Delay Time | | $t_{d(off)}$ | $R_G$=3.9Ω | - | 57 | - | |
| Fall Time | | $t_f$ | $V_{GS}$=10V | - | 50 | - | |
| **Gate Charge Characteristics**[Note7] | | | | | | | |
| Gate to Source Charge | | $Q_{gs}$ | $V_{GS}$=100V | - | 22 | - | nC |
| Gate to Drain Charge | | $Q_{gd}$ | $V_{DS}$=10V | - | 12 | - | |
| Gate Charge Total | | $Q_g$ | $I_D$=50A | - | 62 | - | |
| **Reverse Diode Characteristics** | | | | | | | |
| Drain-Source Diode Forward Voltage | | $V_{SD}$ | $V_{GS}$=0V, $I_{SD}$=50A | - | 0.8 | 1.2 | V |
| Reverse Recovery Time[Note7] | | $t_{rr}$ | $I_{SD}$=50A $V_{GS}$=0V | - | 133 | - | ns |
| Reverse Recovery Charge[Note7] | | $Q_{rr}$ | di/dt=100A/us | - | 625 | - | nC |

Notes:

1. Single pulse; pulse width ≤100μs.
2. $E_{AS}$ is based on starting $T_J$ = 25°C, L = 0.5mH, $I_{AS}$=72A ,$R_G$ = 25Ω, $V_{GS}$ =10V; 100% FT tested at L = 0.5mH, $I_{AS}$ = 36A.
3. The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance $R_{θJC}$
4. The power dissipation Pdsm is based on Tj(max), using junction-to-case thermal resistance $R_{θJA}$
5. Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
6. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C.
7. Guaranteed by design, not subject to production testing.
8. Pulse width ≤380μs; duty cycle≤2%

# Typical Performance Characteristics

Figure 1: Typ. Output Characteristics

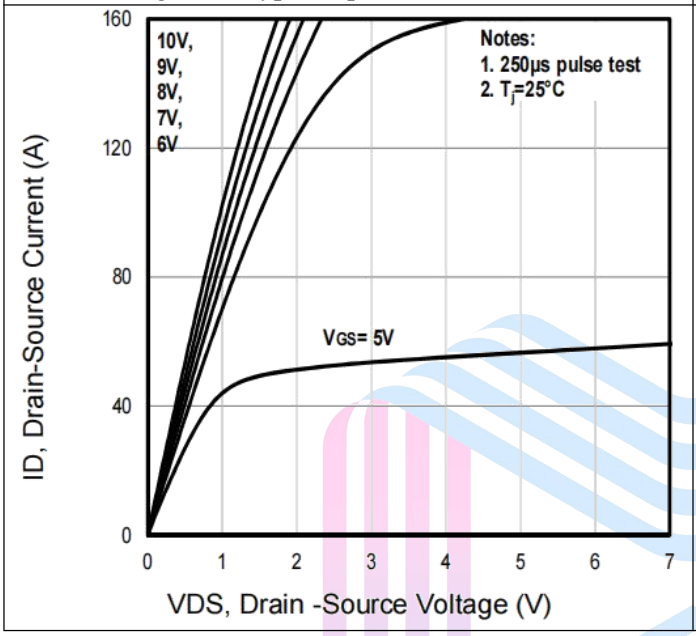



Figure 2: Typ. Gate Charge

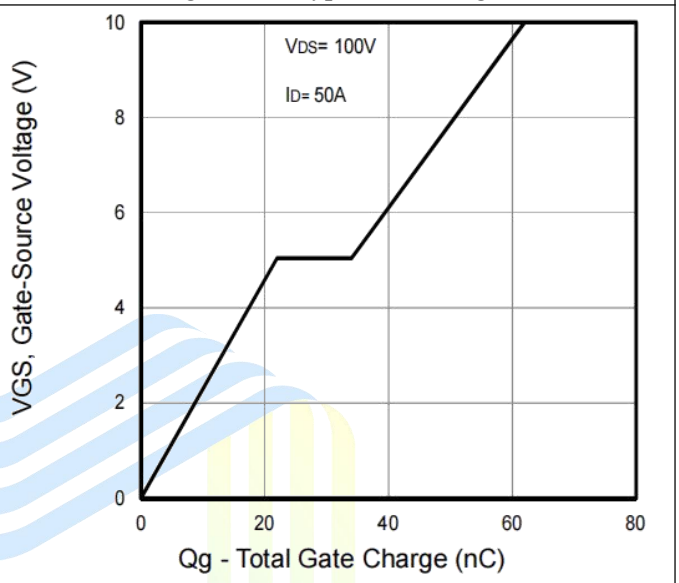



Figure 3: Normalized On-State Resistance

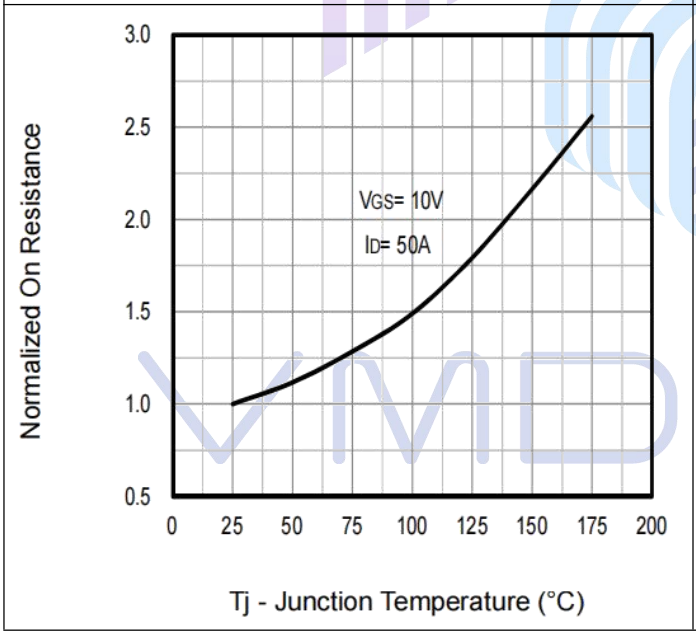



Figure 4: Typ. Transfer Characteristics

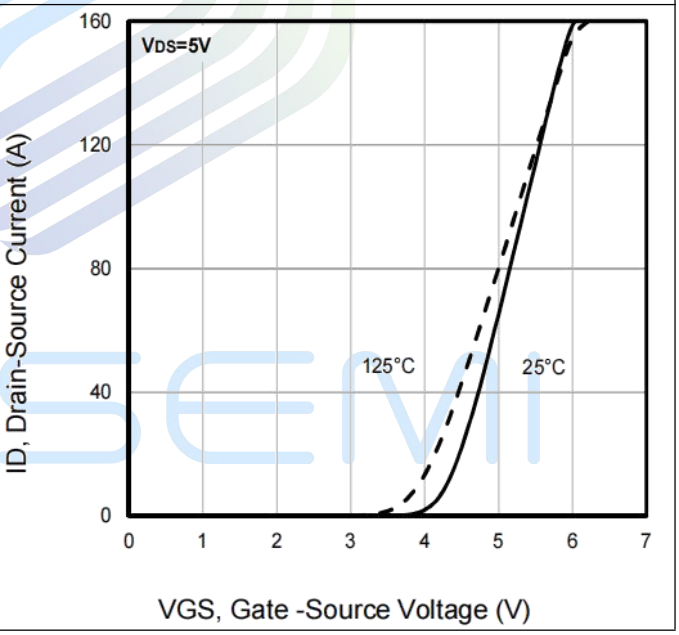


Figure 5: Typical On Resistance vs $V_{GS}$

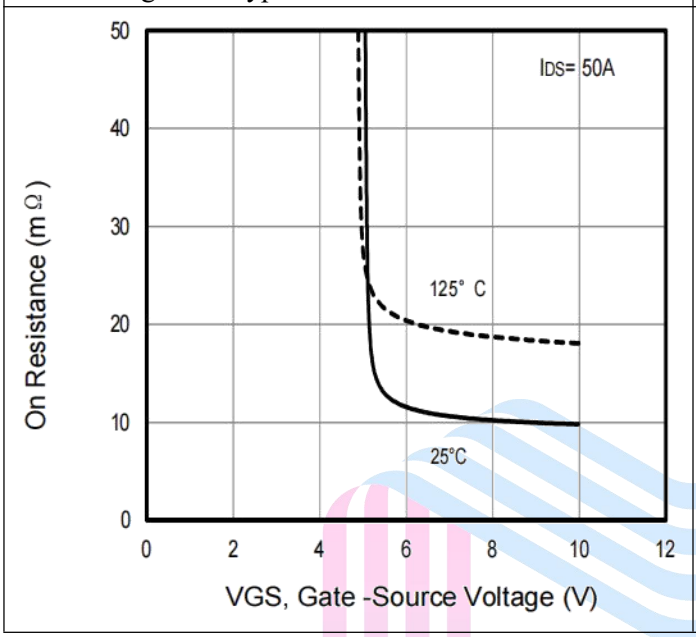



Figure 6: Typical On Resistance vs $I_D$ and $V_{GS}$

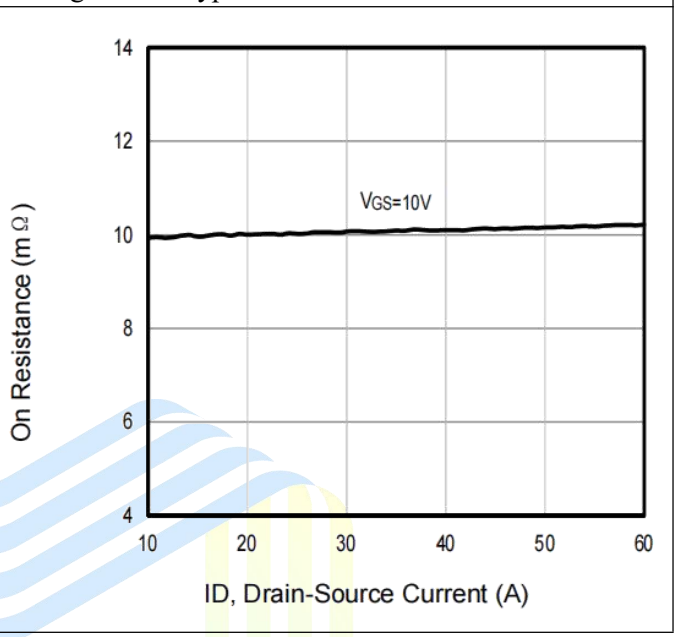



Figure 7: Power Dissipation Vs. Case Temperature

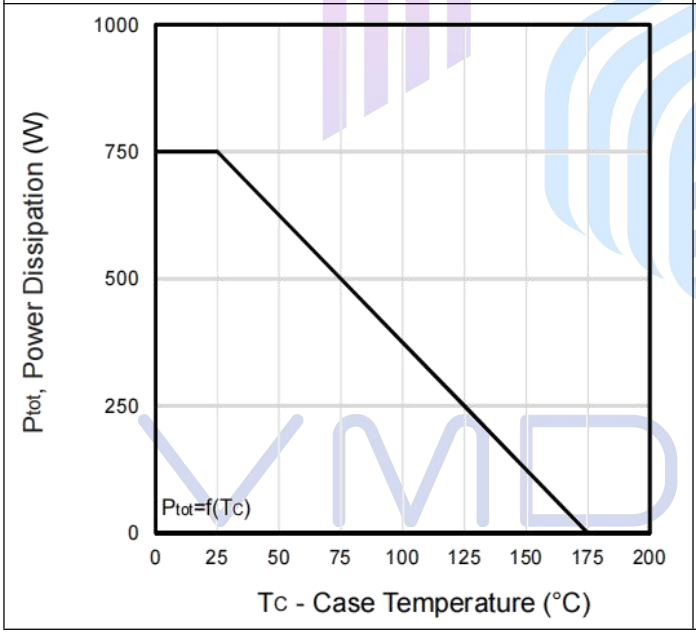



Figure 8: Drain Current Vs. Case Temperature

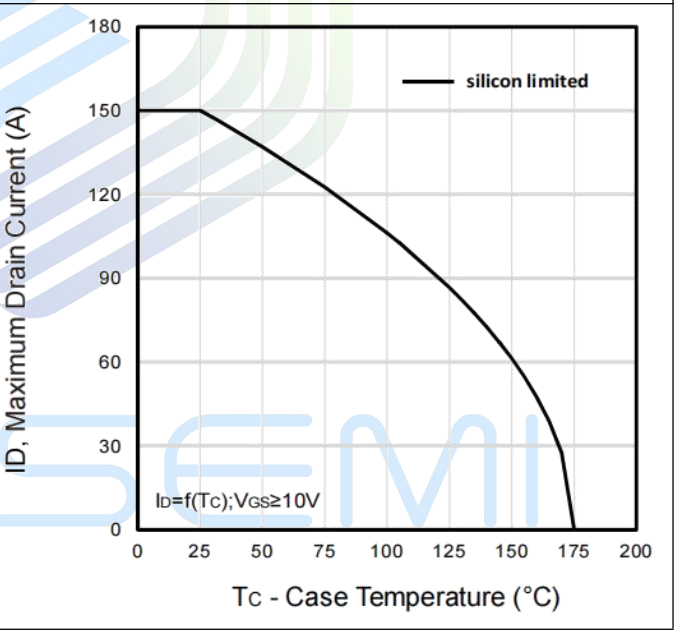


Figure 9: Typ. Capacitances

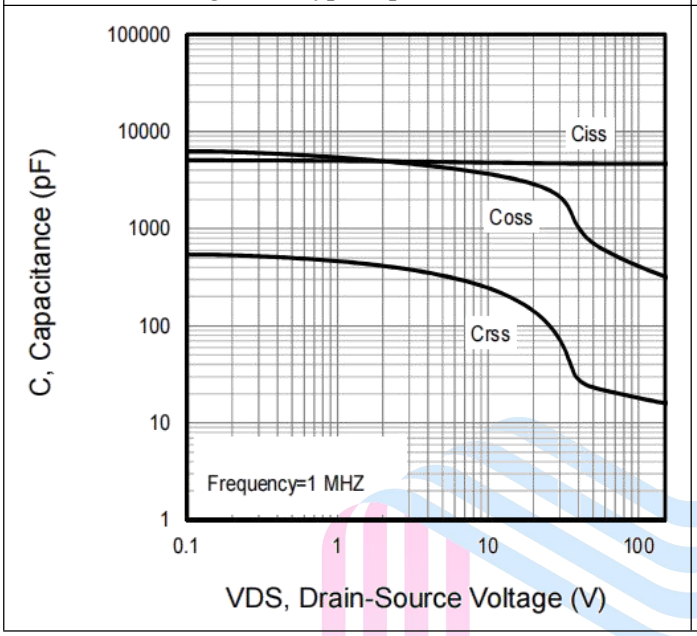



Figure 10: Forward Characteristics of Body Diode

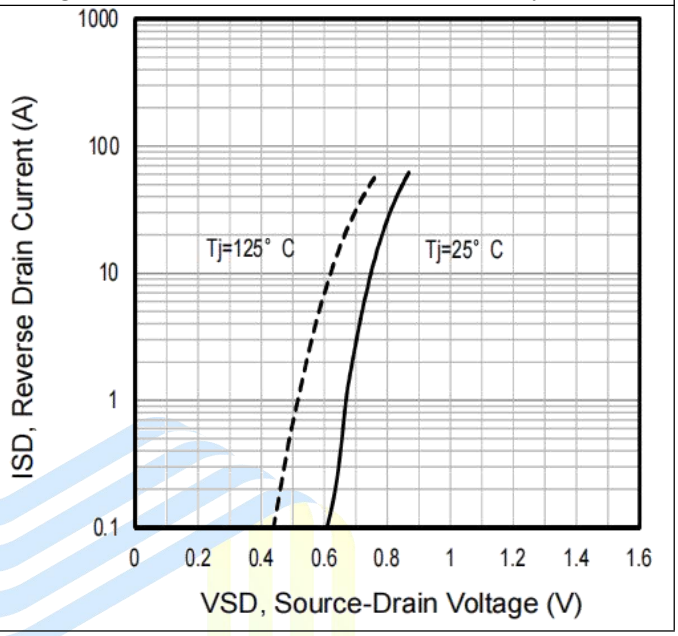



Figure 11: Gate-Source Threshold Voltage

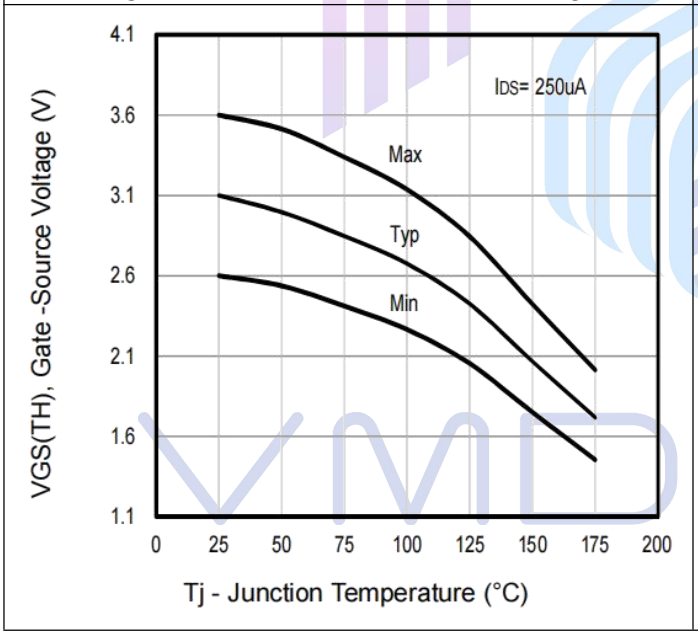



Figure 12: Safe Operating Area

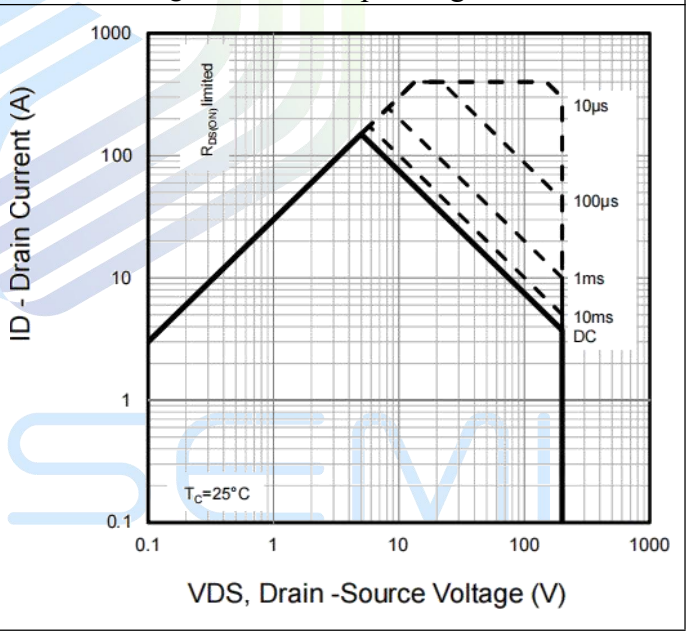
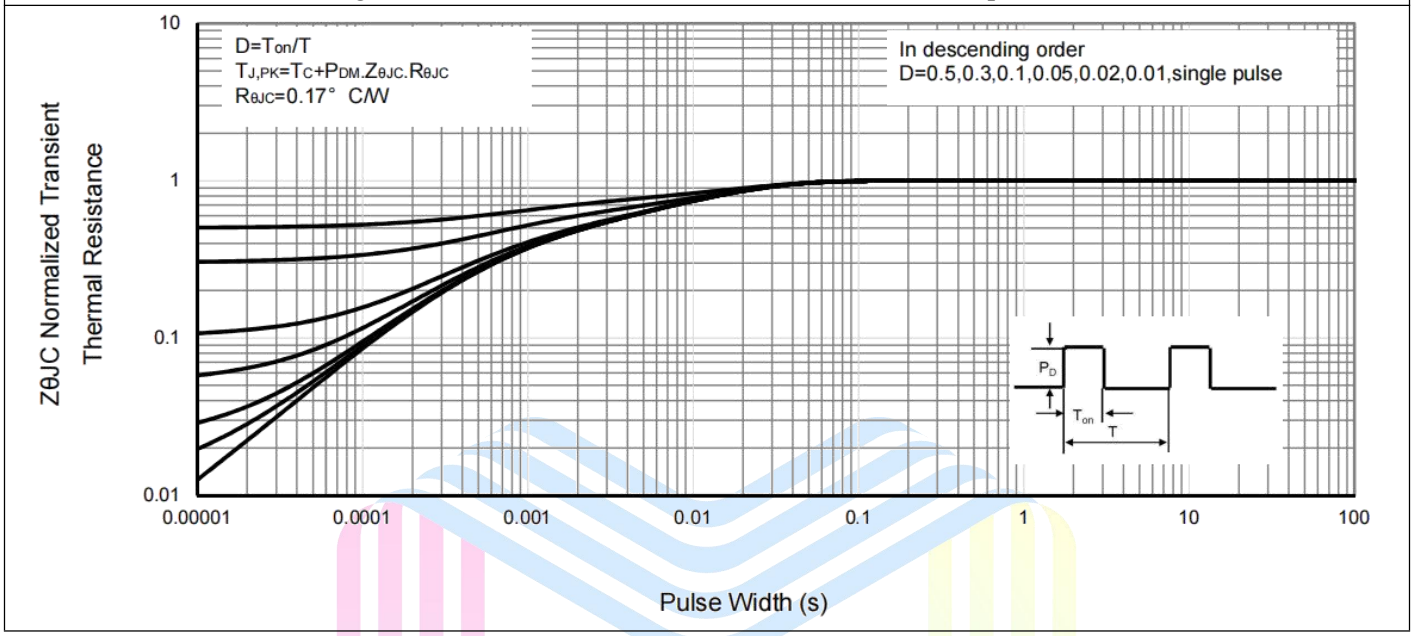
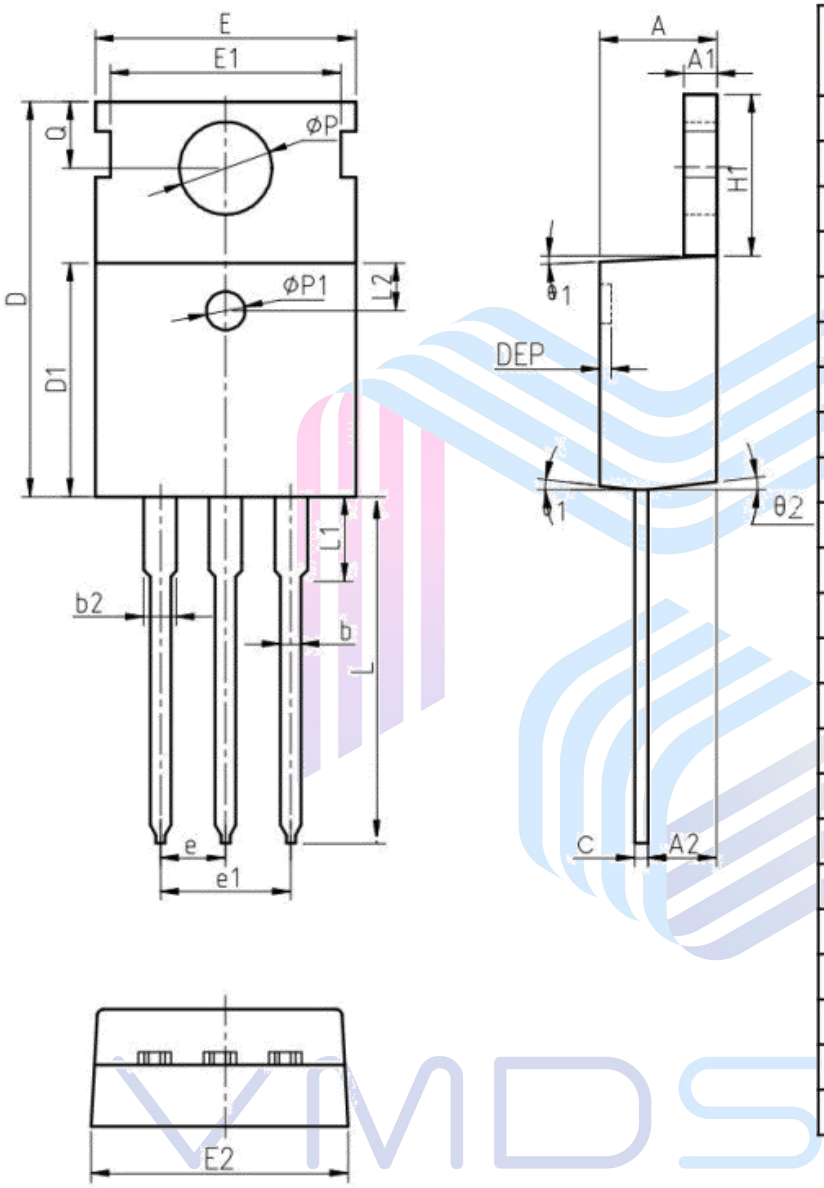


Figure 13: Normalized Maximum Transient Thermal Impedance



# Mechanical Dimensions

**Package Information TO-220**




| Symbol | Dimensions (unit: mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 4.30 | 4.52 | 4.70 |
| A1 | 1.15 | 1.30 | 1.40 |
| A2 | 2.20 | 2.40 | 2.60 |
| b | 0.70 | 0.80 | 1.00 |
| b2 | 1.17 | 1.32 | 1.50 |
| c | 0.45 | 0.50 | 0.61 |
| D | 15.30 | 15.65 | 15.90 |
| D1 | 9.00 | 9.20 | 9.40 |
| DEP | 0.05 | 0.10 | 0.25 |
| E | 9.66 | 9.90 | 10.28 |
| E1 | - | 8.70 | - |
| E2 | 9.80 | 10.00 | 10.20 |
| ΦP1 | 1.40 | 1.50 | 1.60 |
| e | 2.54 BSC | | |
| e1 | 5.08 BSC | | |
| H1 | 6.40 | 6.50 | 6.80 |
| L | 12.70 | - | 14.27 |
| L1 | - | - | 3.95 |
| L2 | 2.40 | 2.50 | 2.60 |
| ΦP | 3.53 | 3.60 | 3.70 |
| Q | 2.70 | 2.80 | 2.90 |
| θ1 | 5 ° | 7 ° | 9 ° |
| θ2 | 1 ° | 3 ° | 5 ° |

Notes:

1. Refer to JEDEC TO-220
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

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