VFO120N10TA1
Datasheet

Description

Low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low Vth series is specially optimized for synchronous rectification systems with low driving voltage.

Applications

- Switching voltage regulator
- PD charger
- Motor driver
- DC-DC convertor
- Switched mode power supply

Features

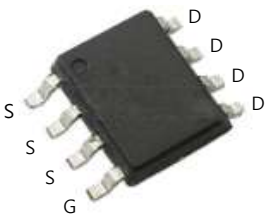
- Low $R_{DS(ON)}$ and FOM
- Extremely Low Switching Loss
- Excellent Reliability and Stability
- Fast switching and soft recovery

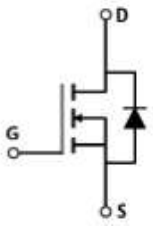
Key Performance Parameters

Parameter	Value	Unit
$V_{DS,min}$ @ $T_{j,max}$	100	V
$R_{DS(on),max}$ @ V_{GS}=10V	12	mΩ
Q_g	24.2	nC
$I_{D,pulse}$	30	A

Packaging and Internal Circuit

Part Name	Package	Marking
VFO120N10TA1	SOP8	VFO120N10TA1





Absolute Maximum Ratings (Tj=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current[1], T_C=25°C	I_D	10	A
Pulsed drain current[2], T_C=25 °C	$I_{D,\ pulse}$	30	A
Continuous diode forward current[1], T_C=25 °C	I_S	10	A
Diode pulsed current[2], T_C=25 °C	$I_{S,\ pulse}$	30	A
Power dissipation[3], T_C=25 °C	P_D	4	W
Single pulsed avalanche energy[5]	E_{AS}	30	mJ
Operation and storage junction temperature	T_{stg}, T_j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-ambient[4]	$R_{\theta JA}$	62.5	°C/W

Static Characteristics (Tj=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	100			V
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A		10	12	mΩ
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=10A		13	20	mΩ
Gate threshold voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.0		2.5	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	μA
Gate-source leakage current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Gate resistance	R_G	f=1 MHz, Open drain		5		Ω

Dynamic Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=100kHz		1379		pF
Output capacitance	C_{oss}			754		pF
Reverse transfer capacitance	C_{rss}			55.2		pF
Turn-on delay time	$t_{d(on)}$	V_{GS}=10V, V_{DS}=50V, R_G=2Ω, I_D=10A		13.5		ns
Rise time	t_r			6.1		ns
Turn-off delay time	$t_{d(off)}$			32.7		ns
Fall time	t_f			7.8		ns

Gate Charge Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gate to source charge	Q_{gs}	V_{GS}=10V, V_{DS}=50V, I_D=10A		4.4		nC
Gate to drain charge	Q_{gd}			5.6		nC
Gate charge total	Q_g			24.2		nC
Gate plateau voltage	$V_{plateau}$			3		V

Body Diode Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_S=12A			1.3	V
Reverse recovery time	t_{rr}	V_R=50V, I_S=10A, di/dt =100A/μs		43.1		ns
Reverse recovery charge	Q_{rr}			80.4		nC
Peak reverse recovery current	I_{rrm}			2.7		A

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
5) V_{DD}=50 V,V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical characteristics diagram

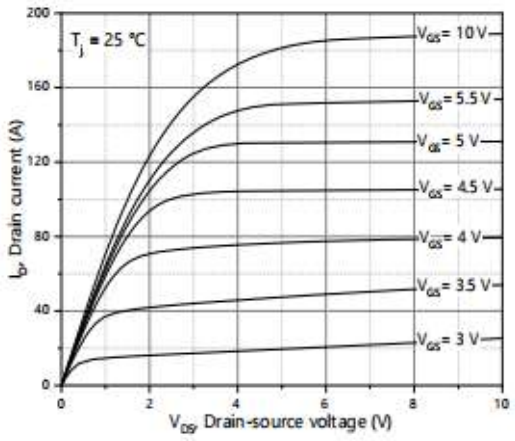
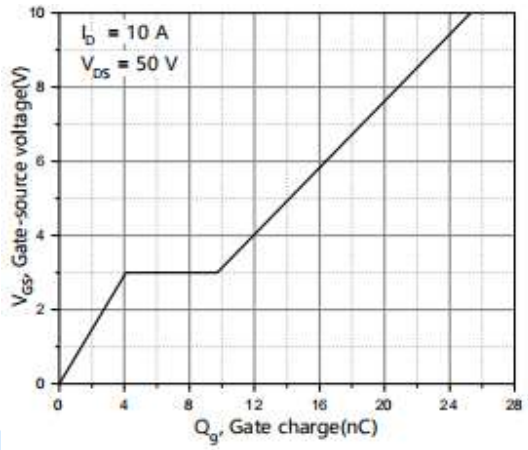
Diagram 1: Typ. output characteristics	Diagram 2: Typ. gate charge
	

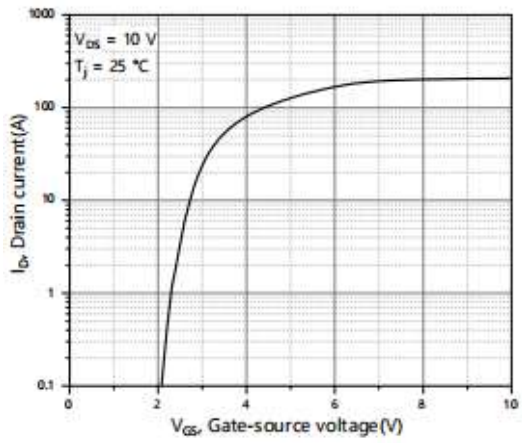
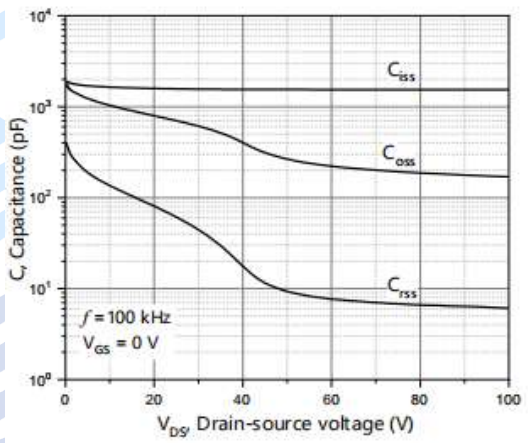
Diagram 3: Typ. transfer characteristics	Diagram 4: Typ. capacitances
	

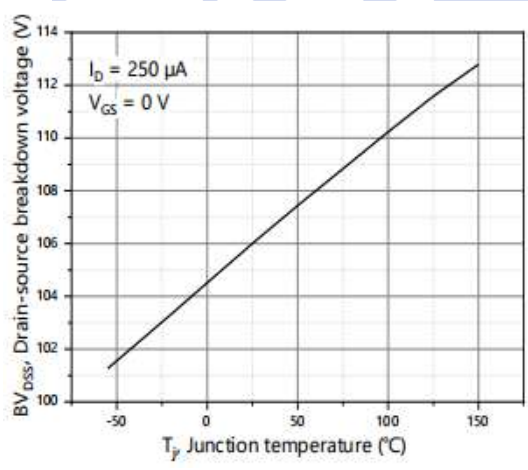
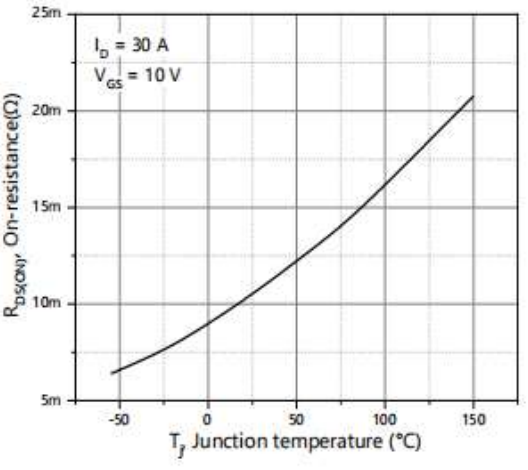
Diagram 5: Drain-source breakdown voltage	Diagram 6: Drain-source on-state resistance
	

Diagram 7: Drain-source on-state resistance

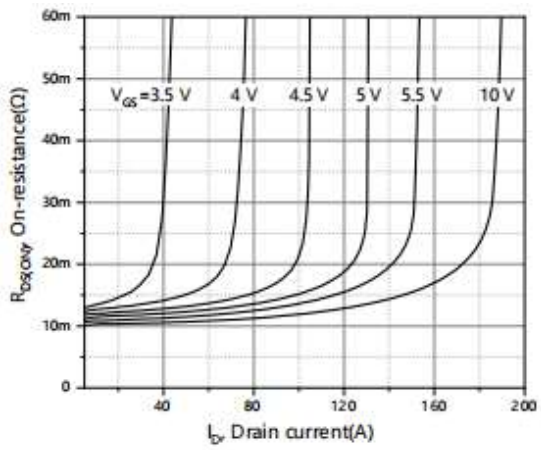


Diagram 8: Forward characteristic of body diode

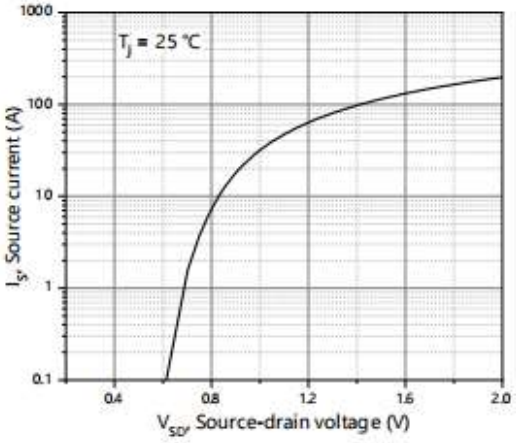
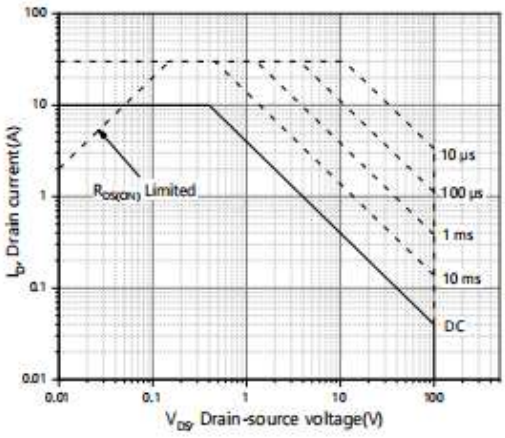


Diagram 9: Safe operation area at T_C=25 °C



Test Circuits and waveforms

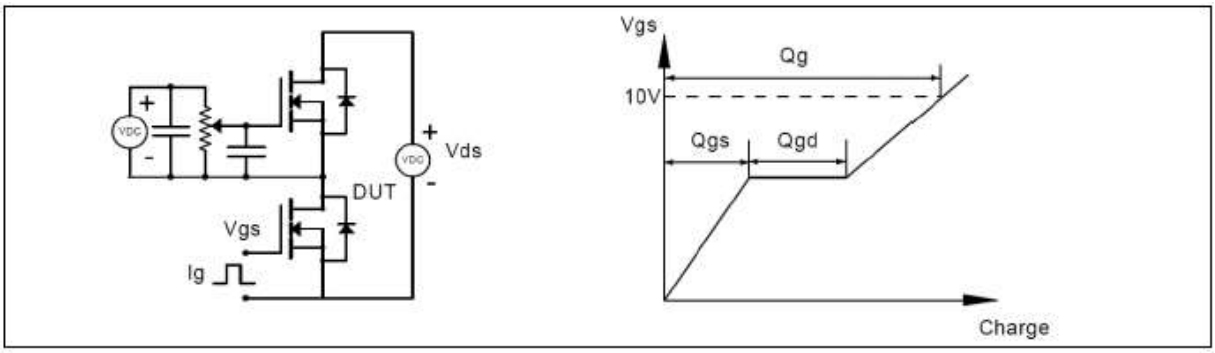


Figure 1. Gate charge test circuit & waveform

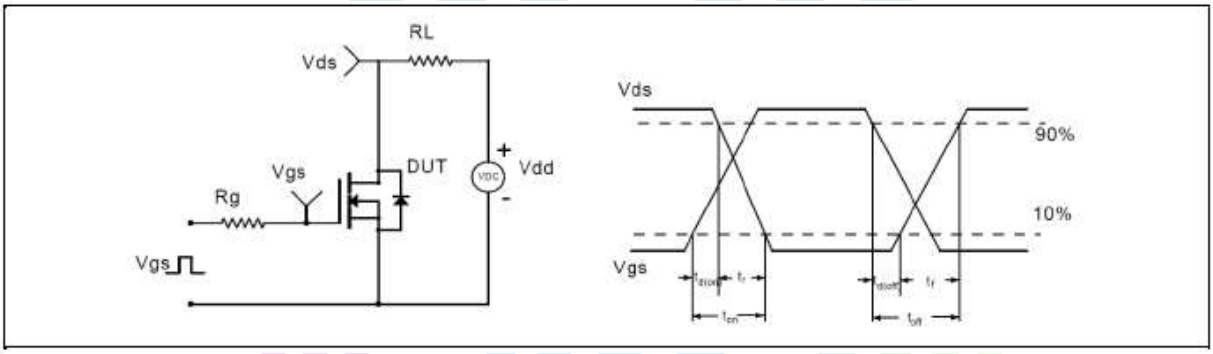


Figure 2. Switching time test circuit & waveforms

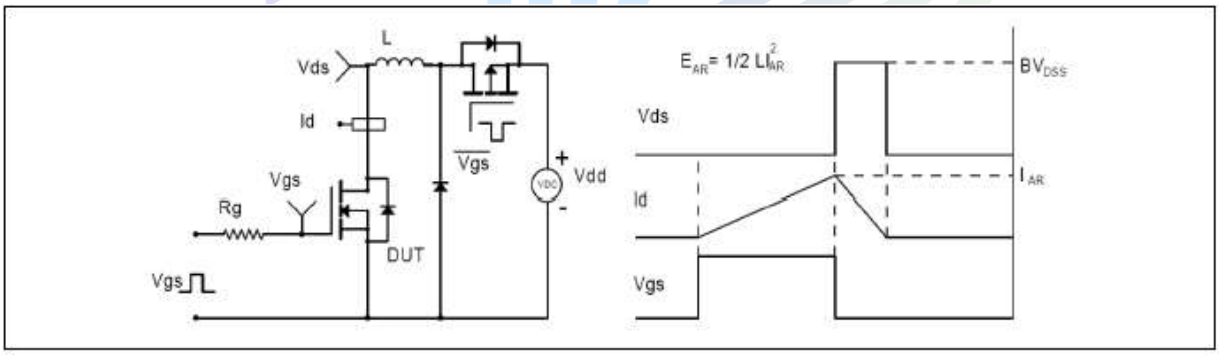


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

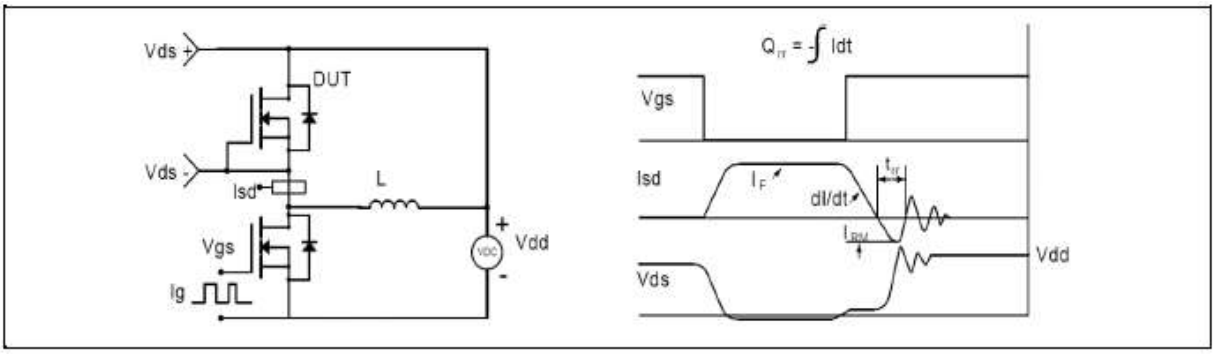
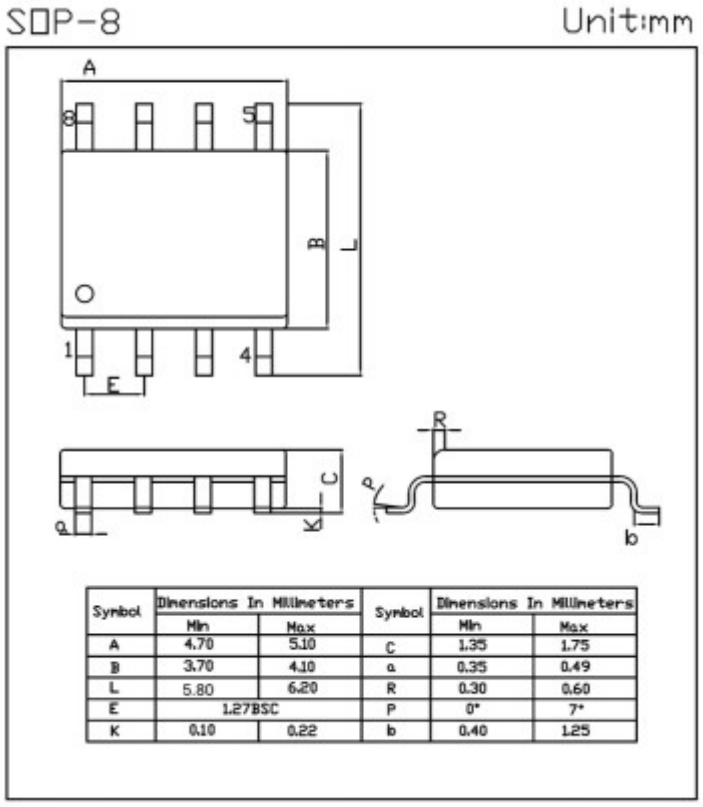


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outlines



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	5.80	6.20	R	0.30	0.60
E	1.27BSC		P	0°	7°
K	0.10	0.22	b	0.40	1.25

Outline SOP8

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2021-05-08	Release version

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