VUDA002R85APA

Datasheet

General Description

VUDA002R85APA MOSFET is based on unique device design to achieve low $R_{DS(ON)}$, ESD Protected Up to 2.0KV (HBM).

Symbol

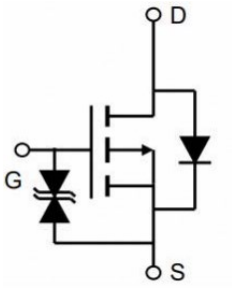


Figure 1 Symbol of VUDA002R85APA

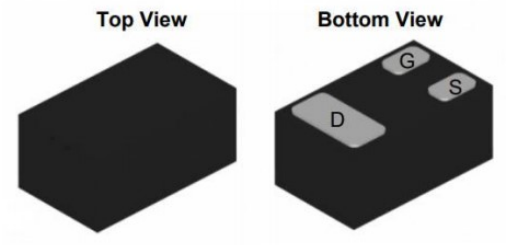
Features

- $R_{DS(ON)\_max}$ = 850.0mΩ@V_{GS} = -4.5V
- $R_{DS(ON)\_max}$ = 1200.0mΩ@V_{GS} = -2.5V
- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching

Application

- Power management
- Interfacing, Logic switch
- Load Switch

Package Type



DFN1006-3L

Figure 2 Package Type of VUDA002R85APA

Ordering Information

Product Name	Package
VUDA002R85APA	DFN1006-3L

Absolute Maximum Ratings (T_A= 25 ºC, unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current	T_A = 25℃@Steady state	I_D	-0.65	A
Continuous Drain Current	T_A = 70℃@Steady state		-0.52	A
Pulsed Drain Current[Note1]		I_{DM}	-2.0	A
Total Power Dissipation	T_A = 25℃	P_D	0.9	W
Junction Temperature		T_J	150	ºC
Storage Temperature		T_{STG}	-55 to 150	ºC

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Ambient [Note2]	$R_{\theta JA}$		138		ºC/W

Notes :

1. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_D is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

Electrical Characteristics (T_J= 25 ºC, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D= -250uA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= -20V, V_{GS}=0V T_C= 25 ºC			-1	uA
Gate-Body Leakage Current	I_{GSS1}	V_{GS} = ±10V, V_{DS}= 0V		±1.5	±10	uA
	I_{GSS2}	V_{GS} = ±8V, V_{DS}= 0V		±0.5	±2	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= -250uA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D= 0.5A		580	850	mΩ
		V_{GS}= -2.5V, I_D= 0.3A		855	1200	
		V_{GS}= -1.8V, I_D= 0.2A		1350	2000	
Dynamic Characteristics Note2						
Input Capacitance	C_{ISS}	V_{DS}= -10V		71		pF
Output Capacitance	C_{OSS}	V_{GS}=0V		20		pF
Reverse Transfer Capacitance	C_{RSS}	f=1MHz		15		pF
Gate Resistance	Rg	f=1 MHz, Open drain		85		Ω
Switching Parameters Note2						
Gate to Source Charge	Q_{gs}	V_{DS}= -10V		0.37		nC
Gate to Drain Charge	Q_{gd}	V_{GS}= -4.5V		0.27		
Gate Charge Total	Q_g	I_D= -0.5A		1.24		
Reverse Recovery Charge	Q_{rr}	I_F= -0.5A		0.97		nC
Reverse Recovery Time	t_{rr}	di/dt=-20A/us		26		ns
Turn-on Delay Time	$t_{d(on)}$	V_{DD}= -10V		4		
Turn-on Rise Time	t_r	V_{GS}= -4.5V		19		
Turn-off Delay Time	$t_{d(off)}$	R_L=2.5Ω		16		
Turn-off Fall Time	t_f	R_{GEN}=3Ω		25		
Diode Characteristics						
Diode Forward Voltage Note3	V_{SD}	V_{GS}=0V, I_S= -0.65A		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-0.65	A

Typical Performance Characteristics

Figure 3: Transfer Characteristics

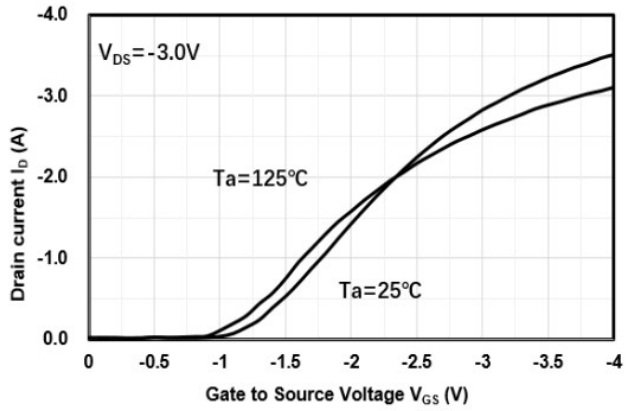


Figure 4: Output Characteristics

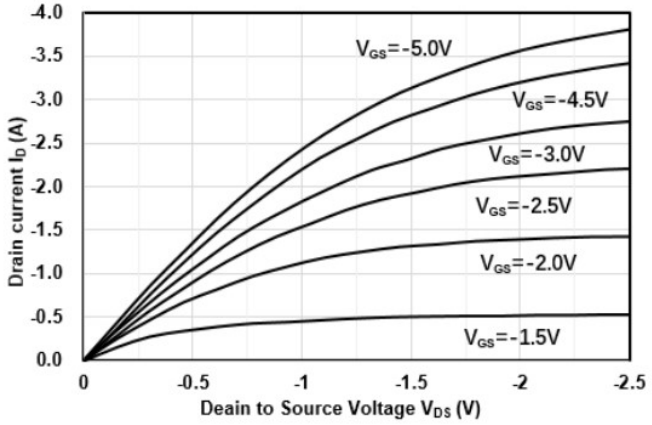


Figure 5: On-Resistance vs. Drain Current and Gate Voltage

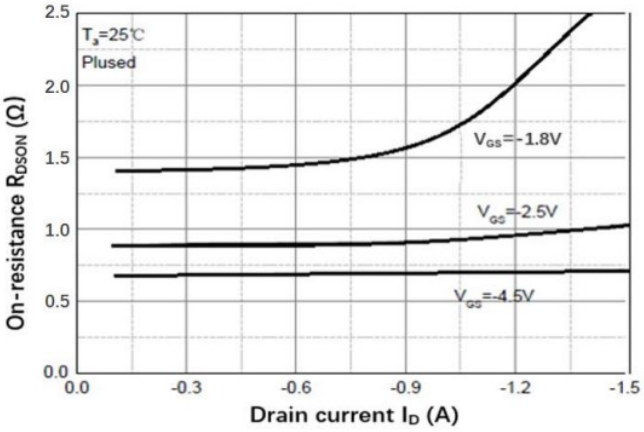


Figure 6: On-Resistance vs. Junction Temperature

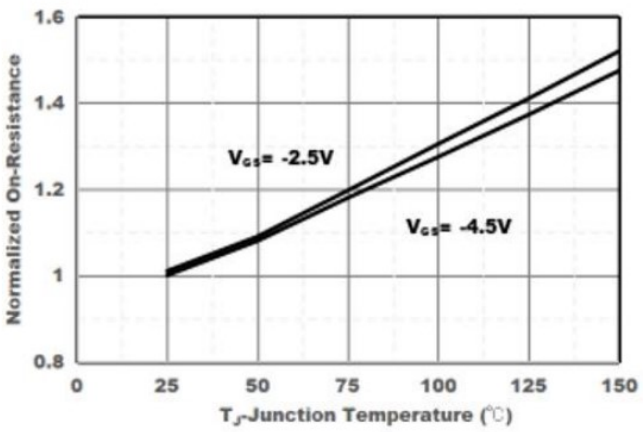


Figure 7: Capacitance Characteristics

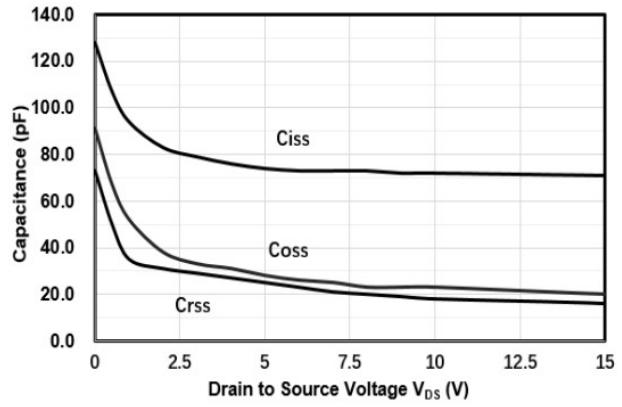


Figure 8: Gate Charge

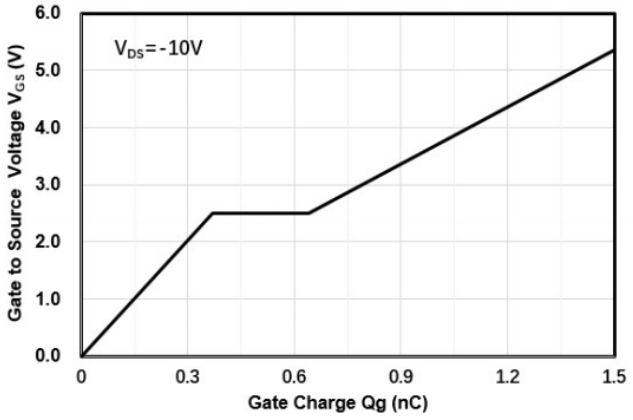


Figure 9: Safe Operation Area

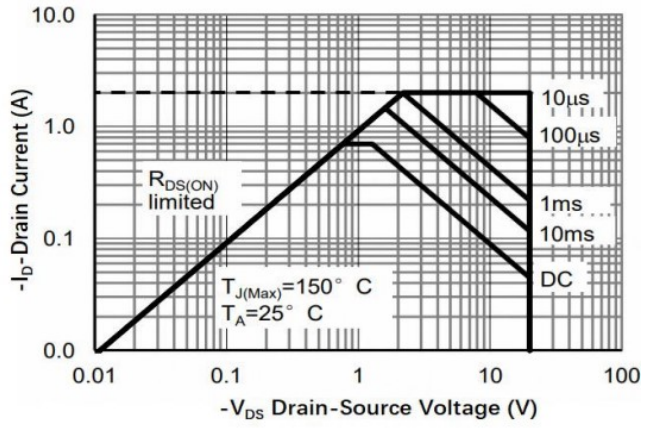


Figure 10: Pulse Power Rating Junction-to-Ambient

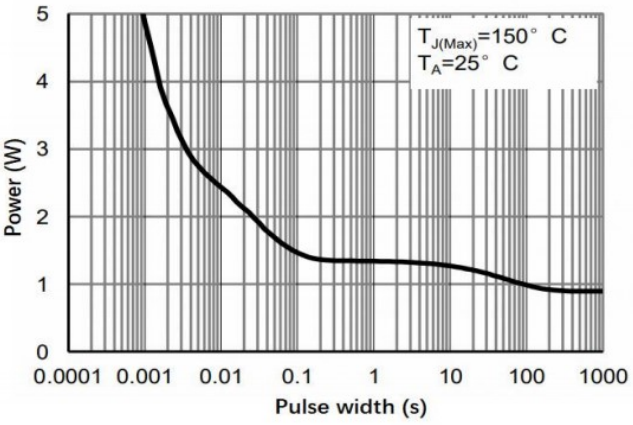
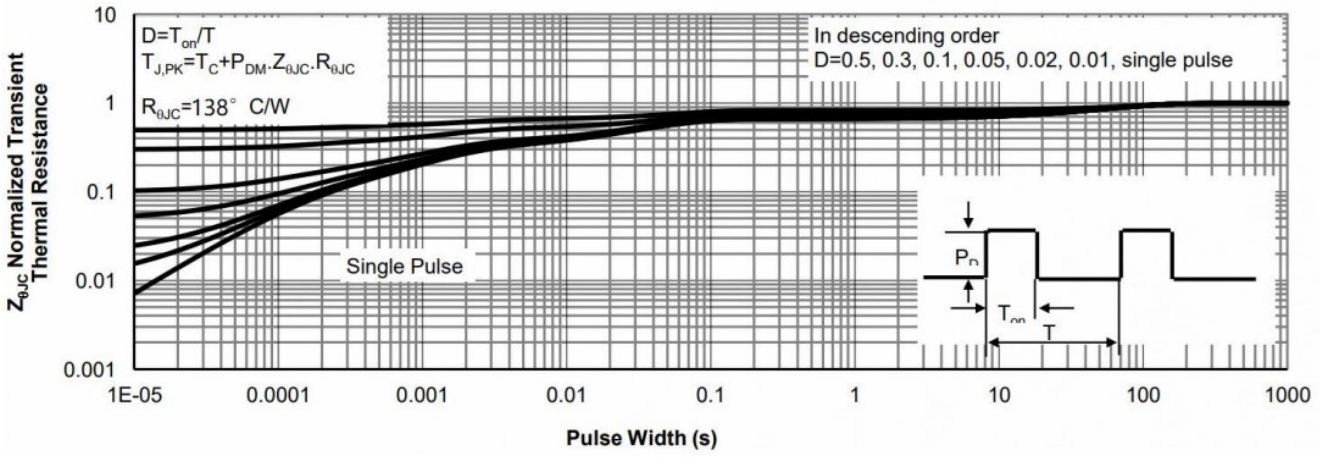
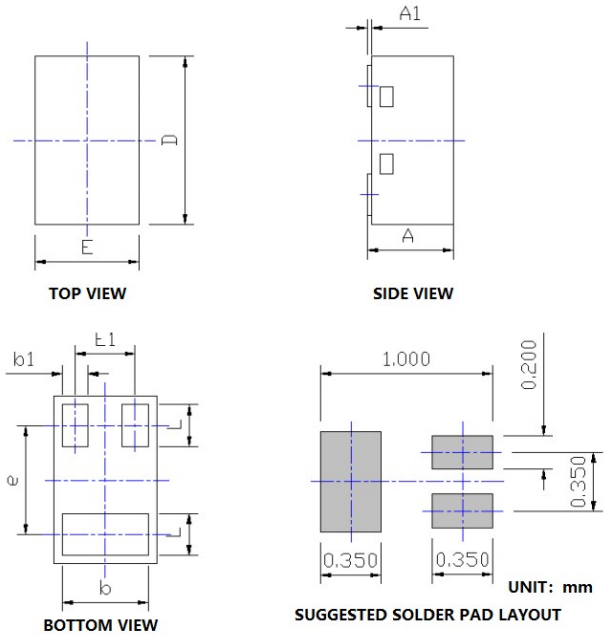


Figure 11: Normalized Maximum Transient Thermal Impedance



Mechanical Dimensions:



Symbol	Dimensions (Unit:mm)		
	Min.	TYP.	Max.
A	0.42	--	0.55
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L1	0.20	0.25	0.30

Note:

1. Package body sizes exclude lead burrs.
2. Tolerance 0.1mm unless otherwise specified.
3. The pad layout is for reference purposes only.

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