



VMDSEMI

VUTS010R055NA

Datasheet



VMDSEMI

General Description

$V_{(BR)DSS}$	$R_{DS(ON)_{max}}$	I_D
100V	5.5mΩ@10V	200A

Symbol

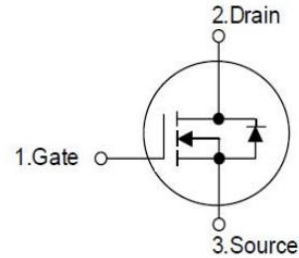


Figure 1 Symbol of VUTS010R055NA

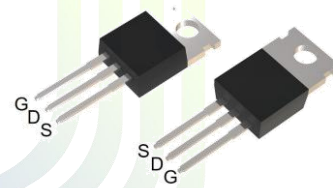
Features

- Low $R_{DS(ON)}$
- 100% Avalanche Tested
- Pb-free lead plating;
- RoHS compliant

Application

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC converter
- Switched mode power supply

Package Type



TO-220AB

Figure 2 Package Type of VUTS010R055NA

VMDSEMI

Ordering Information

Product Name	Package
VUTS010R055NA	TO-220AB

Absolute Maximum Ratings ($T_A=25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	± 25	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	I_D	200	A
Continuous Drain Current	$T_C=100^\circ\text{C}$		142	A
Pulsed Drain Current ^{Note 2}	$T_C=25^\circ\text{C}$	$I_{D,pulse}$	800	A
Continuous Diode Forward Current	$T_C=25^\circ\text{C}$	I_S	200	A
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_{DSM}	15	A
Continuous Drain Current	$T_A=70^\circ\text{C}$		12	A
Max Power Dissipation	$T_C=25^\circ\text{C}$	P_D	375	W
Max Power Dissipation ^{Note 3}	$T_A=25^\circ\text{C}$	P_{DSM}	2	W
Avalanche Energy, Single Pulse ^{Note 4}		E_{AS}	900	mJ
Operation and storage temperature		T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		0.4	0.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		62.5	75	



Electrical Characteristics($T_J = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			1	μA
Zero Gate Voltage Drain Current $T_J = 125\text{ }^\circ\text{C}$		$V_{DS}=100V, V_{GS}=0V$			100	μA
Gate-Body Leakage Current	Forward	$I_{GSSF}, V_{GS}=25V, V_{DS}=0V$			100	nA
	Reverse	$I_{GSSR}, V_{GS}=-25V, V_{DS}=0V$			-100	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.4	3	3.6	V
Drain-Source On-Resistance ^{Note1}	$R_{DS(ON)}$	$V_{GS}=10V, I_D=80A$		4.5	5.5	mΩ
Drain-Source On-Resistance ^{Note1} $T_J = 100\text{ }^\circ\text{C}$				6.5		
Gate resistance	R_G	$f=1\text{ MHz, Open drain}$	0.2	2.3	5	Ω
Dynamic Characteristics						
Input Capacitance	C_{ISS}	$V_{DS}=30V$	11065	14755	19625	pF
Output Capacitance	C_{OSS}	$V_{GS}=0V$	500	665	885	
Reverse Transfer Capacitance	C_{RSS}	$f=1\text{ MHz}$	370	495	660	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=50V$		35		ns
Rise Time	t_r	$I_D=40A$		67		
Turn-off Delay Time	$t_{d(off)}$	$R_G=3\Omega$		128		
Fall Time	t_f	$V_{GS}=10V$		64		
Gate Charge Characteristics						
Gate to Source Charge	Q_{gs}	$V_{GS}=10V$		59	78	nC
Gate to Drain Charge	Q_{gd}	$V_{DS}=50V$		60	90	
Gate Charge Total	Q_g	$I_D=40A$		232	309	
Reverse Diode Characteristics						
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=80A$		0.9	1.2	V
Reverse Recovery Time	t_{rr}	$I_{SD}=40A, V_{GS}=0V$		44	88	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$		77	154	nC

Notes:

- Pulse width $\leq 380\mu s$; duty cycle $\leq 2\%$.
- Repetitive rating; pulse width limited by max junction temperature.
- The power dissipation P_{DSM} is based on $R_{\theta JA}$ and $@T_J = 150\text{ }^\circ\text{C}$.
- Limited by T_{Jmax} , starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.5\text{ mH}$, $R_G = 25\Omega$, $I_{AS} = 60A$, $V_{GS} = 10V$.

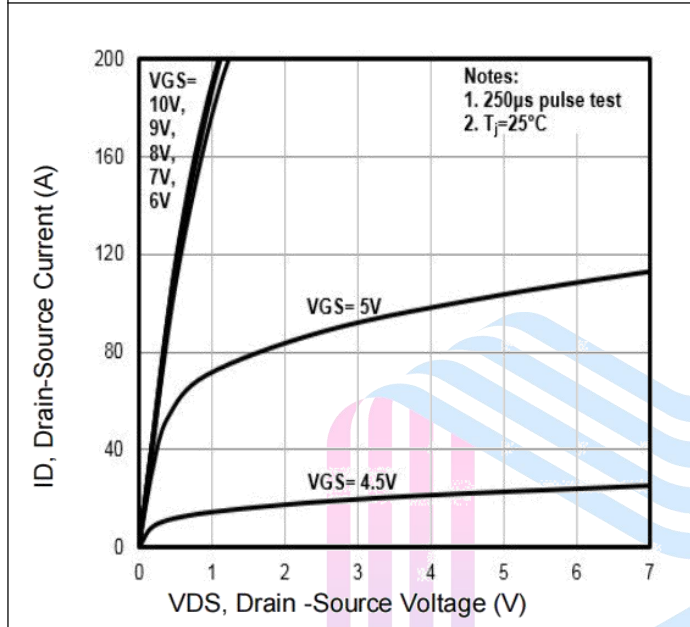
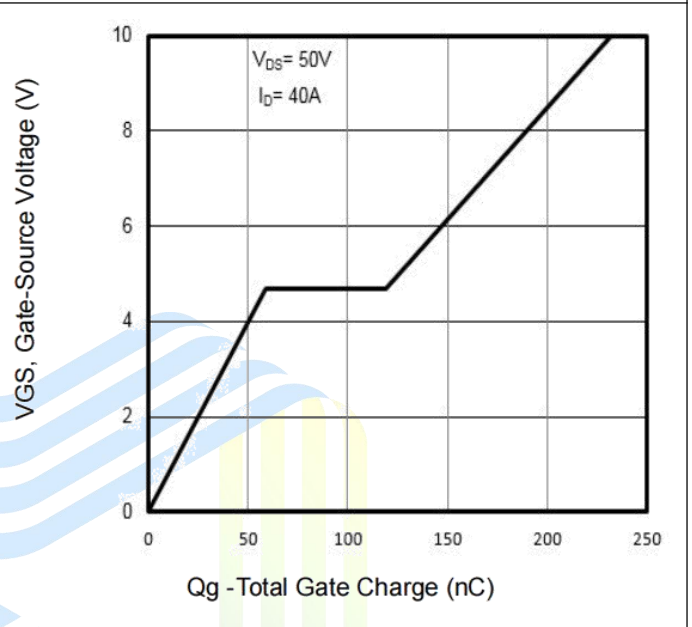
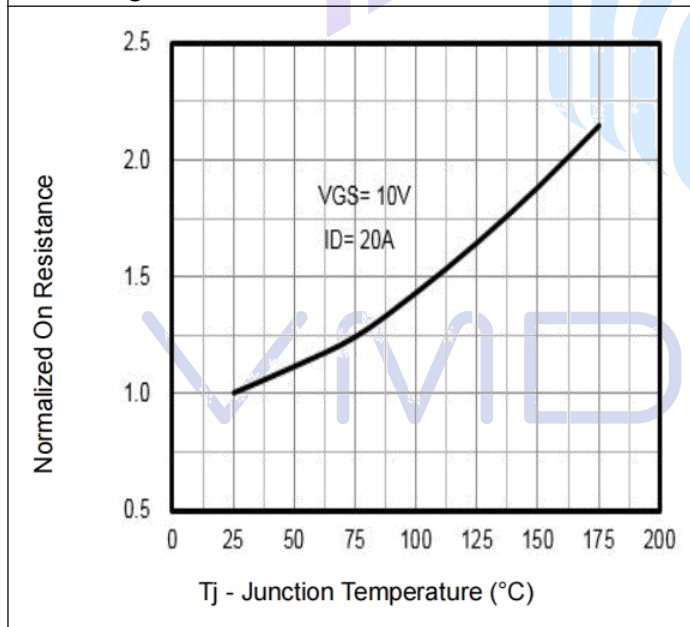
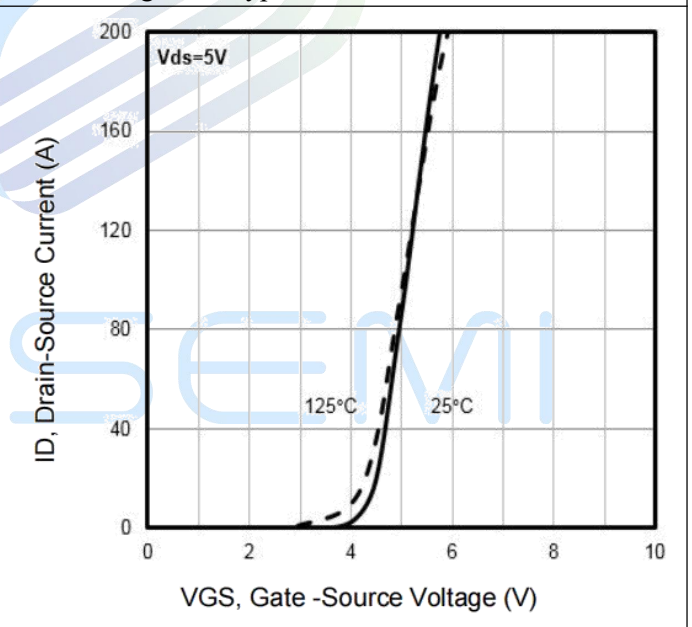
Typical Performance Characteristics
Figure 3: Typ. Output Characteristics

Figure 4: Typ. Gate Charge

Figure 5: Normalized On-State Resistance

Figure 6: Typ. Transfer Characteristics


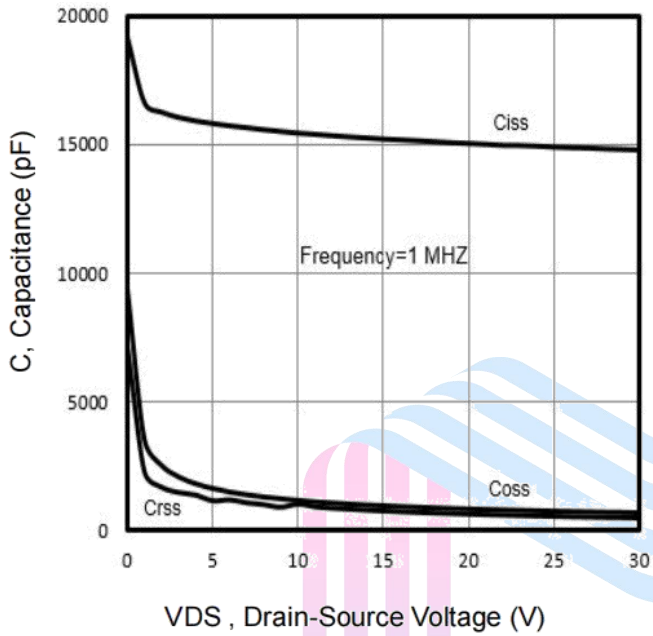
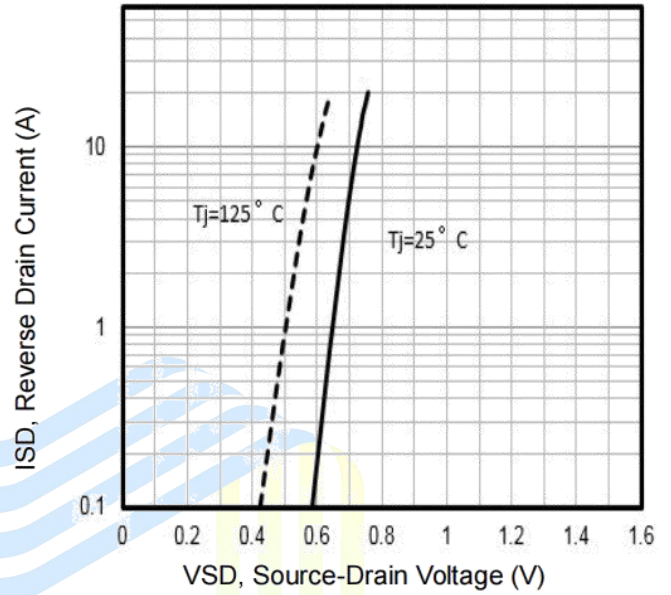
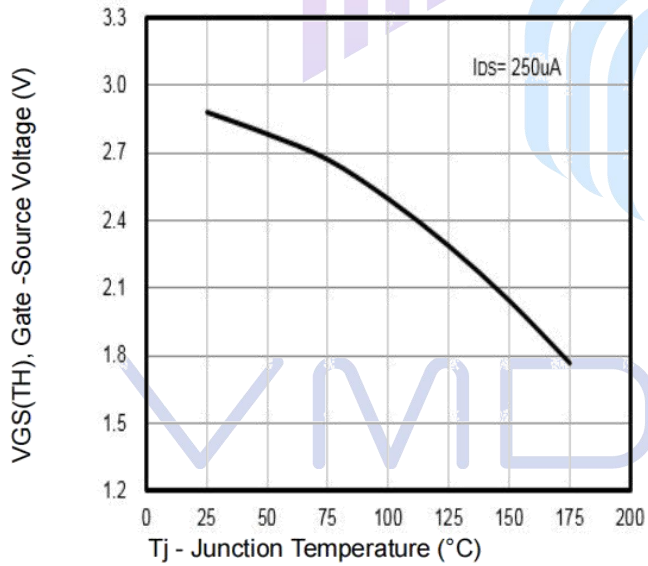
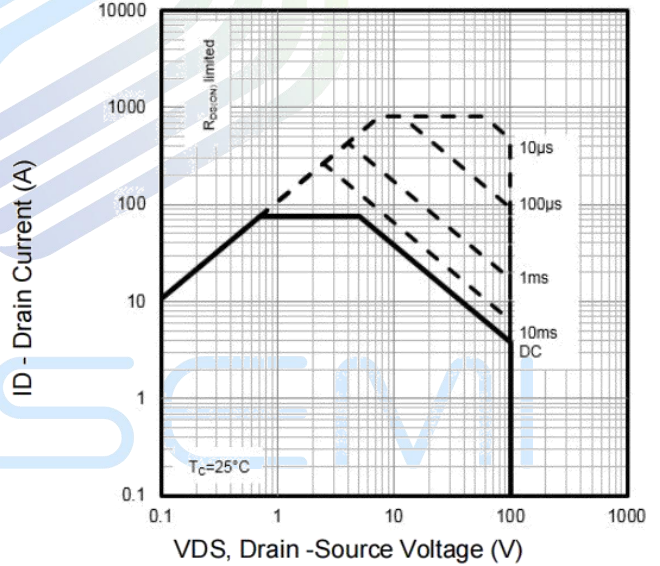
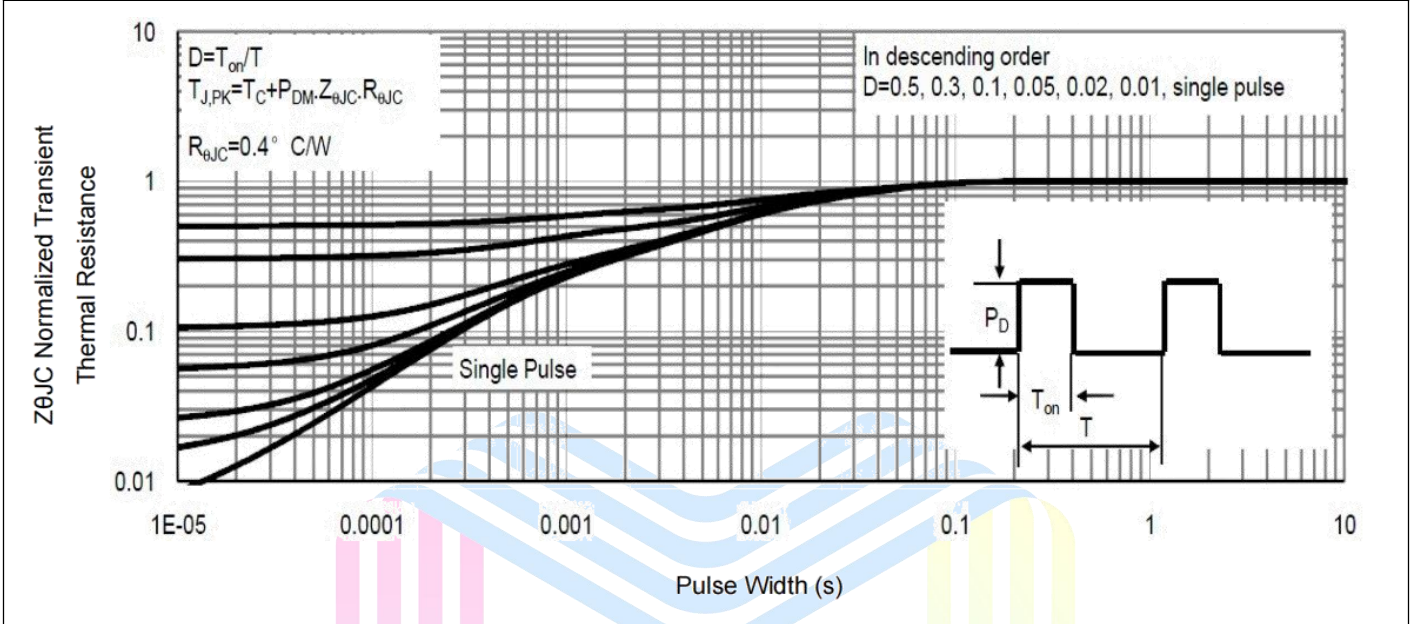
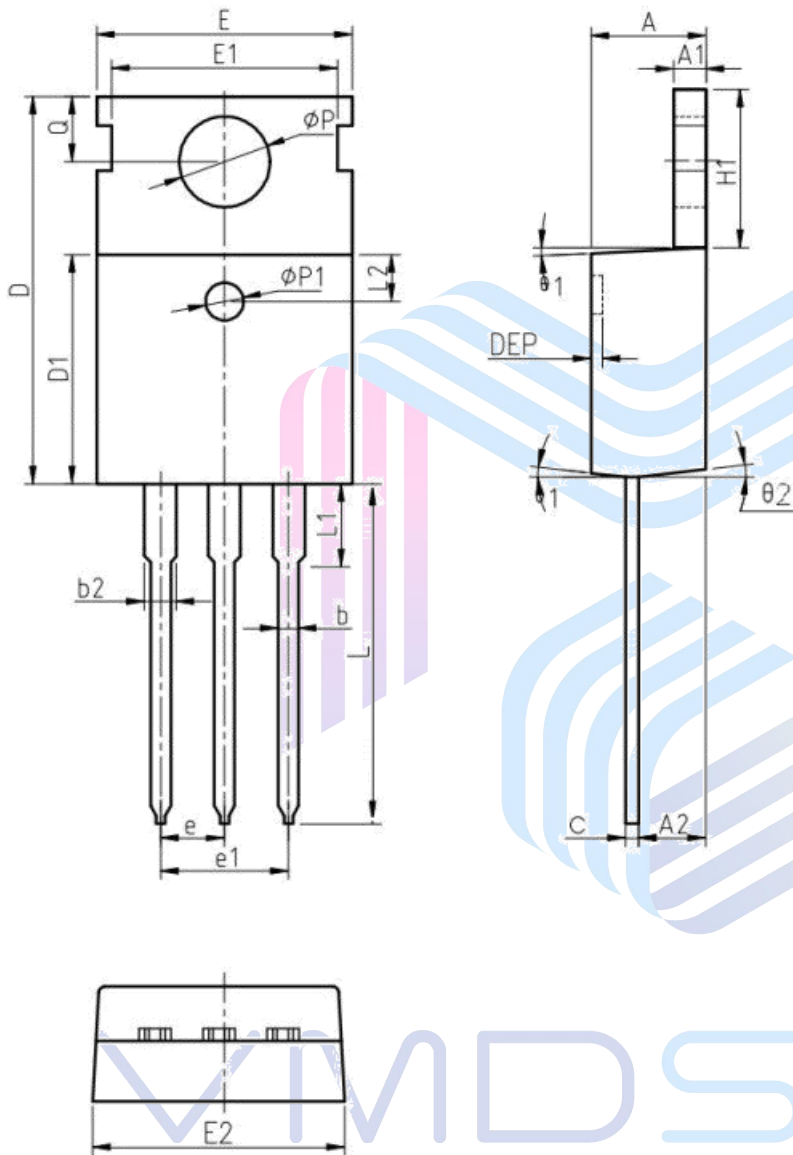
Figure 7: Typ. Capacitances

Figure 8: Forward Characteristics of Body Diode

Figure 9: Gate-Source Threshold Voltage

Figure 10: Safe Operating Area


Figure 11: Normalized Maximum Transient Thermal Impedance




Mechanical Dimensions

Package Information TO-220AB



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
$\phi P1$	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
ϕP	3.53	3.60	3.70
Q	2.70	2.80	2.90
θ_1	5 °	7 °	9 °
θ_2	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

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