VUDD002R130NA

Datasheet

General Description

VUDD002R130NA MOSFET is based on unique device design to achieve low $R_{DS(ON)}$.

Symbol

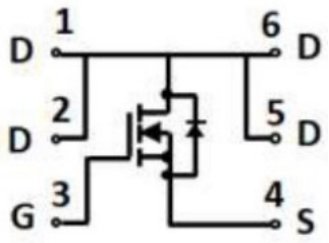


Figure 1 Symbol of VUDD002R130NA

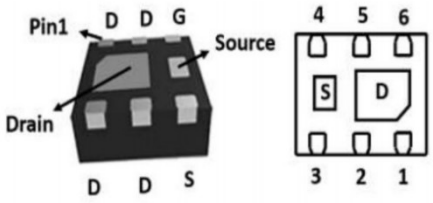
Features

- $R_{DS(ON)\_max}$ = 13.0mΩ@V_{GS} = 4.5V
- $R_{DS(ON)\_max}$ = 16.0mΩ@V_{GS} = 2.5V
- Trench Power LV MOSFET technology
- High Power and Current handing capability

Application

- Power switching application
- Load Switch

Package Type



DFN2X2-6L

Figure 2 Package Type of VUDD002R130NA

Ordering Information

Product Name	Package
VUDD002R130NA	DFN2X2-6L

Absolute Maximum Ratings (T_A= 25 ºC, unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	±10	V
Continuous Drain Current T_A = 25℃	I_D	12	A
Continuous Drain Current T_A = 70℃		9.6	A
Pulsed Drain Current[Note1]	I_{DM}	50	A
Total Power Dissipation T_A = 25℃	P_D	2.5	W
Total Power Dissipation T_A = 70℃		1.6	W
Junction Temperature	T_J	150	ºC
Storage Temperature	T_{STG}	-55 to 150	ºC

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Ambient [Note2]	$R_{\theta JA}$		50		ºC/W

Notes :

1. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%. These parameters have no way to verify.
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Electrical Characteristics (T_J= 25 ºC, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D= 250uA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 20V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	I_{GSS1}	V_{GS} = ±10V, V_{DS}= 0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 4.5V, I_D= 5A		10	13	mΩ
		V_{GS}= 2.5V, I_D= 3A		12.5	16	
		V_{GS}= 1.8V, I_D= 2A		17	25	
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}= 10V		777		pF
Output Capacitance	C_{OSS}	V_{GS}=0V		164		pF
Reverse Transfer Capacitance	C_{RSS}	f=1MHz		140		pF
Switching Parameters						
Gate to Source Charge	Q_{gs}	V_{DS}= 10V		2.8		nC
Gate to Drain Charge	Q_{gd}	V_{GS}= 4.5V		4.6		
Gate Charge Total	Q_g	I_D= 5.6A		25.5		
Reverse Recovery Charge	Q_{rr}	I_F= 0.5A		0.4		nC
Reverse Recovery Time	t_{rr}	di/dt=20A/us		14.4		ns
Turn-on Delay Time	$t_{d(on)}$	V_{DD}= 10V		4.4		
Turn-on Rise Time	t_r	V_{GS}= 4.5V		28.2		
Turn-off Delay Time	$t_{d(off)}$	R_L= 1.5Ω		16.2		
Turn-off Fall Time	t_f	R_{GEN}=3Ω		26		
Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S= 5A			1.2	V

Typical Performance Characteristics

Figure 3: Transfer Characteristics

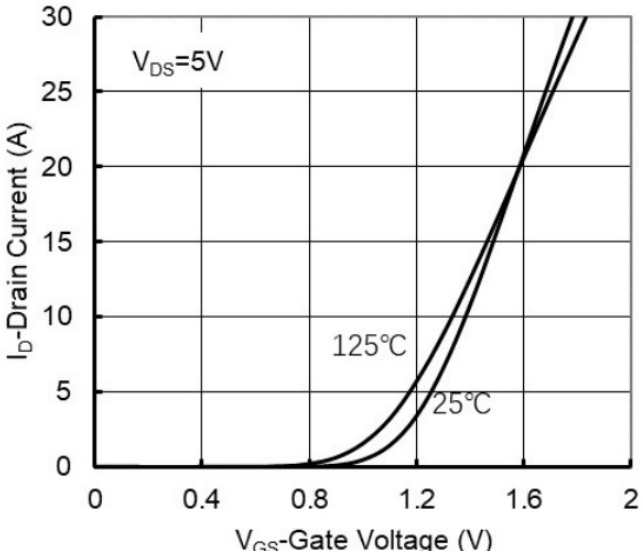


Figure 4: Output Characteristics

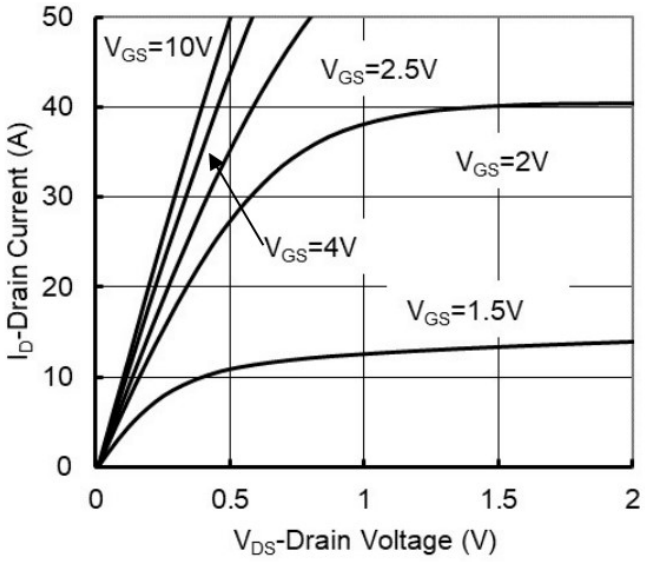


Figure 5: On-Resistance vs. Drain Current and Gate Voltage

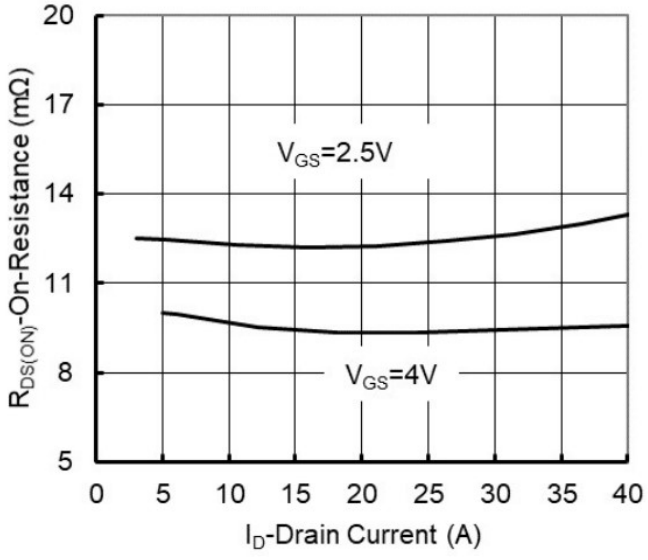


Figure 6: On-Resistance vs. Junction Temperature

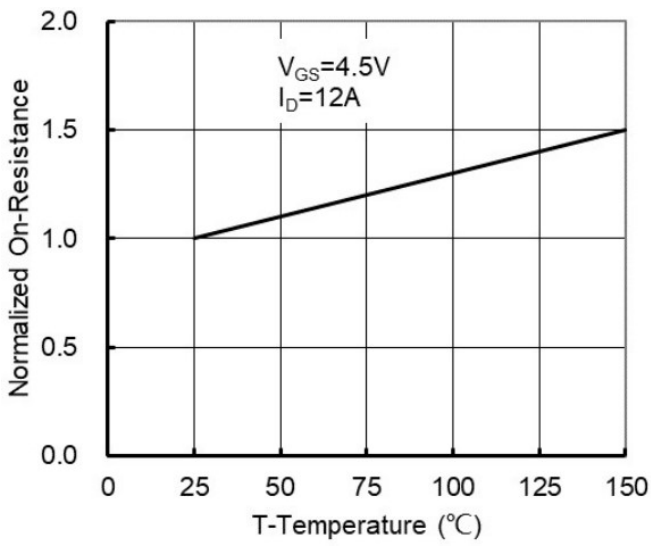


Figure 7: Capacitance Characteristics

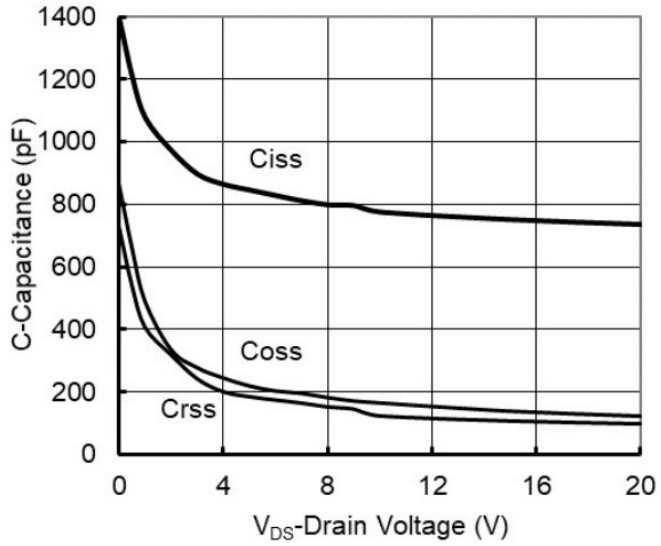


Figure 8: Gate Charge

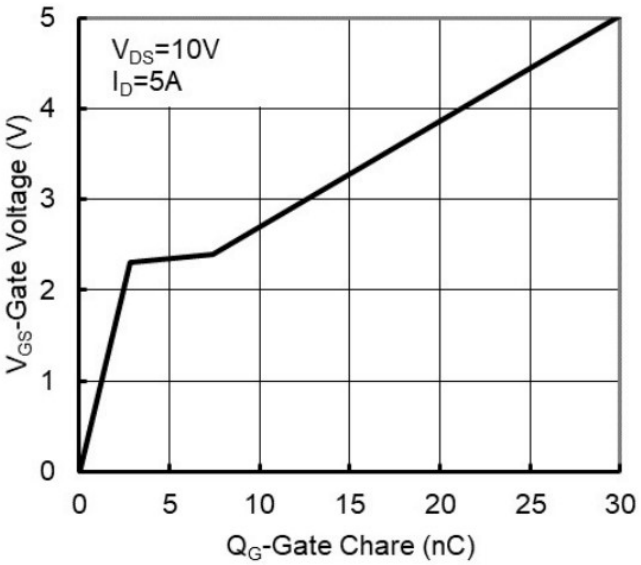


Figure 9: Safe Operation Area

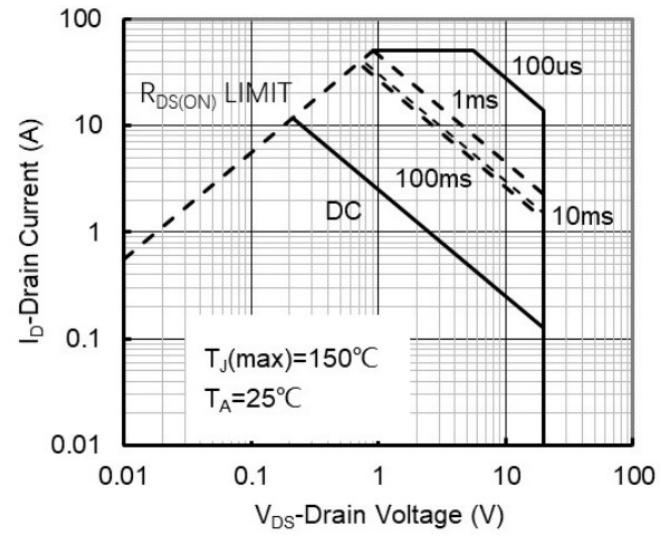


Figure 10: Maximum Continuous Drain Current vs Ambient Temperature

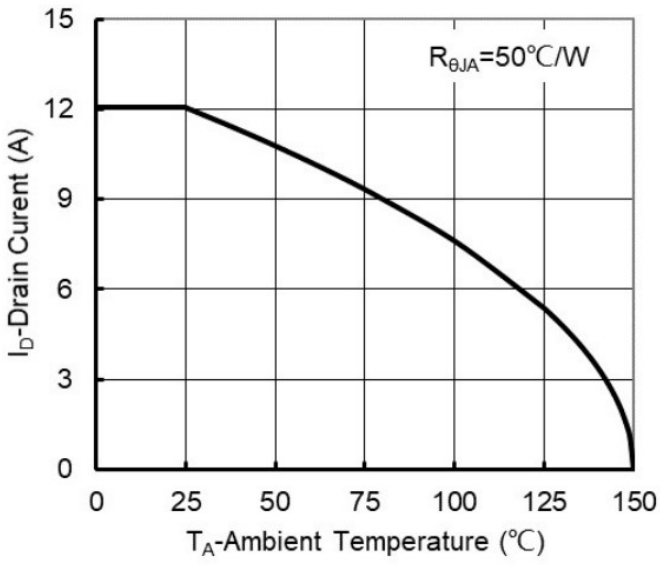
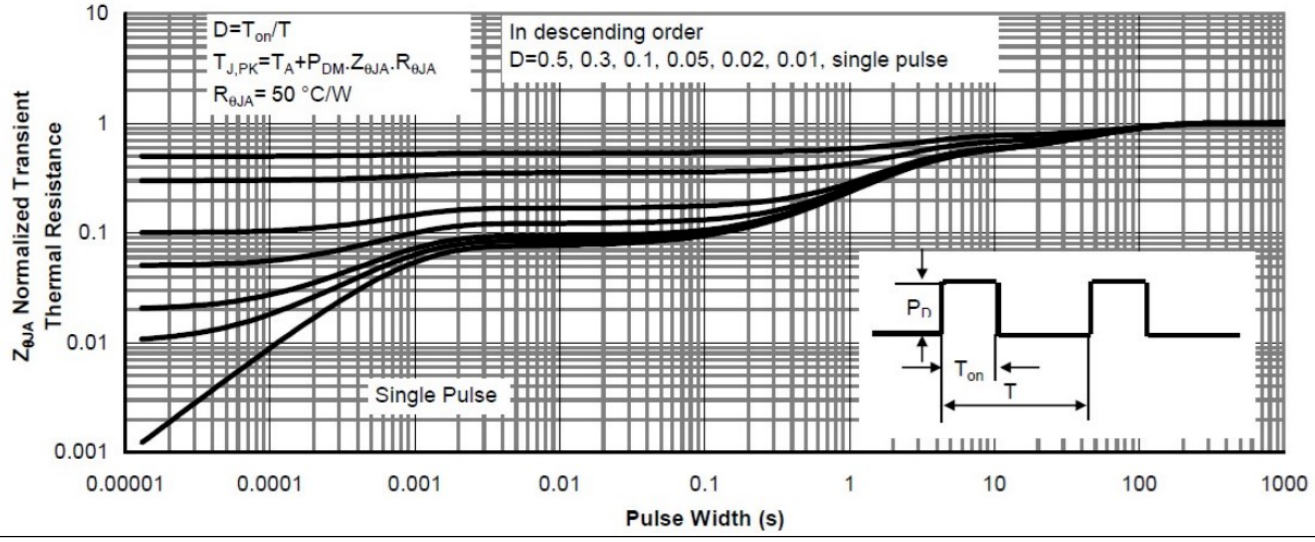
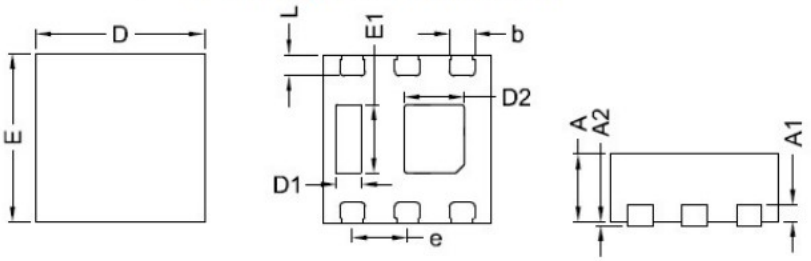


Figure 11: Normalized Maximum Transient Thermal Impedance



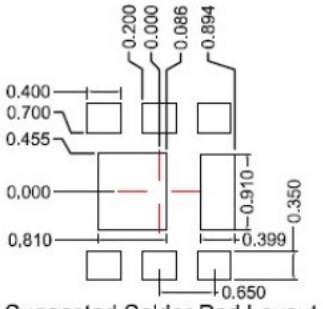
Mechanical Dimensions:

■ DFN2x2-6L Package Information



Top View 正面视图 Bottom View 背面视图 Side View 侧面视图

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

Symbol	Dimensions (Unit:mm)		
	Min.	TYP.	Max.
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65BSC		

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